Firmware development for the first level trigger of ATLAS LAr Calorimeter

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Introduction

The ATLAS Liquid Argon (LAr) calorimeter is one of critical component for ATLAS physics achievement, i.e. the discovery of $H \rightarrow \gamma\gamma$. In order to cope with high luminosity LHC run in the future, enforcement of the calorimeter trigger performance is essential for new physics search. Here the readout electronics system developed toward the Phase-I upgrade (2018 – 2020) is presented.

The new trigger readout scheme

The new scheme so-called Super Cell, will be introduced in order to measure EM (electromagnetic) shower shape at trigger level..

Trigger Tower scheme

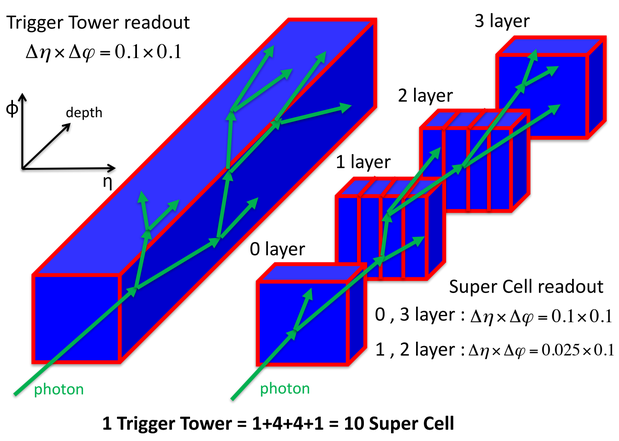
$\Delta\eta\times\Delta\phi = 0.1\times0.1$

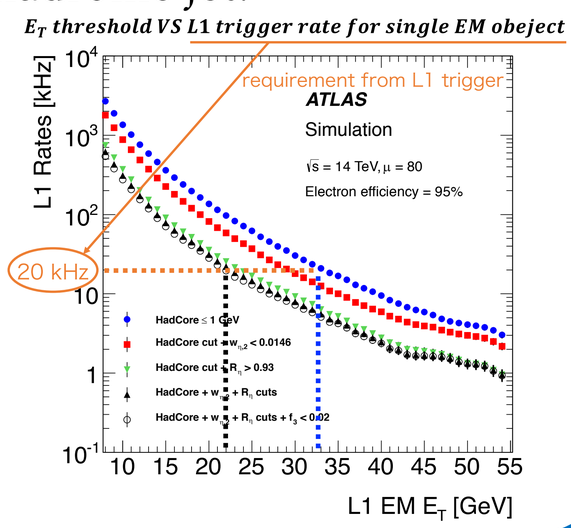
Super Cell scheme

0, 3 layer : $\Delta\eta\times\Delta\phi = 0.1\times0.1$
1, 2 layer : $\Delta\eta\times\Delta\phi = 0.025\times0.1$

1 Trigger Tower = 1 + 4+4+1 = 10 Super Cell

The new trigger readout (Black point) can decrease the energy threshold than the current one (Blue point), because it provides better energy resolution and the shower information which enhances the separation capability between electron, photon and hadronic jet.





Upgrade of the readout electronics

Tokyo group is working for the Backend electronics.

LDPB (LAr Digital Processing Blade)

Main role

- Convert ADC data of each Super Cell (~34k) into E_T.
- Identify the bunch crossing of the significant energy.

Requirement

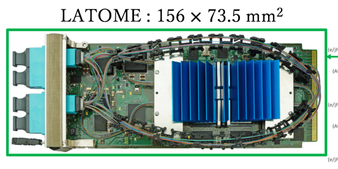
- The latency of signal processing is less than 125 ns.
- Transferred to L1Calo at ~ 50 Tbps.

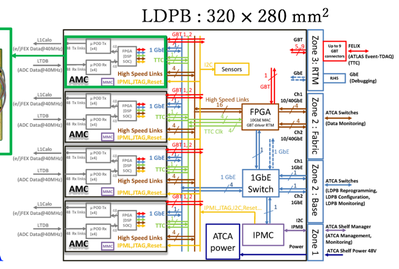
31 LDPBs installed in three ATCA crates.
4 AMCs so-called LATOME in one LDPB.
→ The total of 124 LATOME is used.

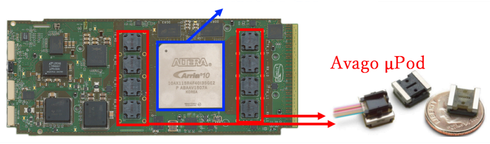
Transceiver speed
~11.2 Gbps/fiber → ~ 450 Gbps/LATOME

Challenging!

LATOME Board
- 4 pairs of μPod
- 96 optical fibers
- Arria10 FPGA
- 156 × 73.5 mm²







Signal Processing

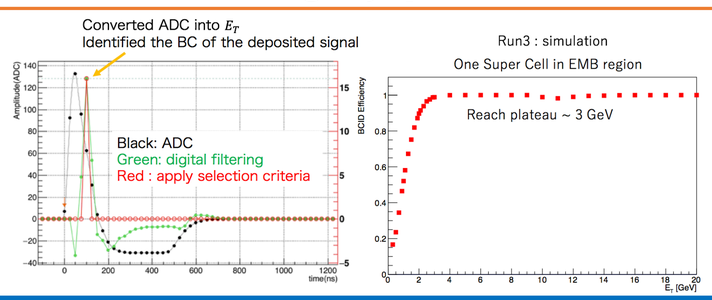
Digital filtering — FIR Filter

$$E_T = \sum_{i=1}^{4} a_i (S_i - P)\,, E_T\tau = \sum_{i=1}^{4} b_i\,(S_i - P)$$

Selection criteria

$$|\tau| < \begin{cases} 8\,ns : -1\,GeV \le E_T < 10\,GeV \\ 2\,ns :\ 10\,GeV \le E_T \end{cases}$$

S_i: ADC data, P: pedestal, a_i, b_i : coefficient, τ : Timing of pulse



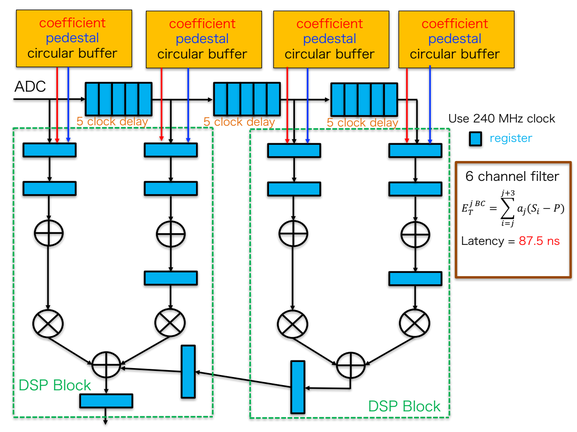
Firmware development

Each FPGA takes care of 320 Super Cells.
→ Serialize 6 Super Cell with 62 parallel processing with 240 MHz.

Core processing block: 6 channel serialized FIR Filter.

- Use circular buffer RAM to correspond to 6 channel.
- All calculation is done in DSP Block in FPGA.
  →Improve F_{max} and latency.

FIR Filter firmware result
- Total latency : 87.5 ns
- F_{max} : 257.6 MHz
- DSP Block usage ratio : 16 %



All results are satisfied with the requirement.

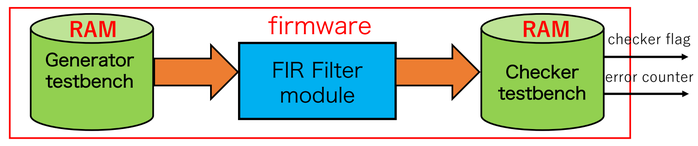
Summary and Prospect

Tokyo group has been working on Phase-I upgrade for ATLAS LAr calorimeter in order to enhance performance of the calorimeter trigger. The FPGA firmware on LATOME AMC is developed, which calculates the transverse energy with a fixed latency. We have established the first version of firmware fulfilling all requirements, and confirmed stable running in the hardware test. The prototype hardware will be assembled soon and tested carefully before entering mas-production. All hardware will be verified before installation into ATLAS by the end of 2018, then installed by 2020.

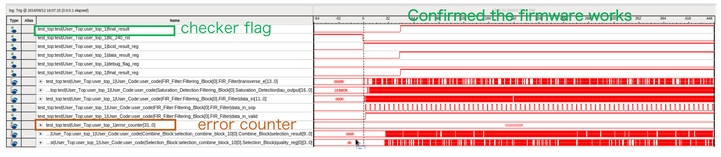
Test result on hardware (LATOME/Dev-Kit)

Tested the firmware for several hours.
- Checker flag = 1
- Error counter = 0

The firmware stably works.



1. Input data (ADC data, coefficient and pedestal) and the calculation result by PC is stored in RAM.
2. Generator testbench provides input data for FIR Filter module.
3. Checker testbench compares the calculation result and firmware result.
   → output "checker flag" and "error counter".



Reference

ATLAS Collaboration, ATLAS LAr Calorimeter Phase-I upgrade TDR, CERN-LHCC-2013-017