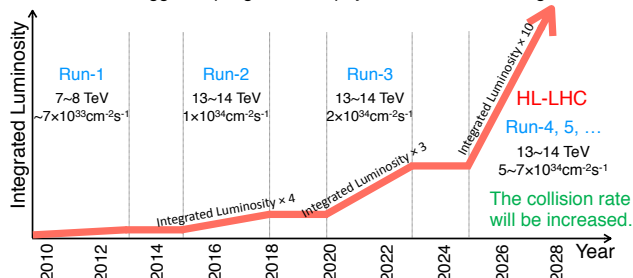# Development of a prototype front-end board of the Thin Gap Chamber for ATLAS at the High-Luminosity LHC

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High-Luminosity LHC (2026~)

Measurement of Higgs coupling and new physics searches with higher statistics.

Run-1
7~8 TeV
~7×10³³cm⁻²s⁻¹

Run-2
13~14 TeV
1×10³⁴cm⁻²s⁻¹

Run-3
13~14 TeV
2×10³⁴cm⁻²s⁻¹

HL-LHC
Run-4, 5, …
13~14 TeV
5~7×10³⁴cm⁻²s⁻¹

The collision rate will be increased.

In order to cope with the higher event rate for HL-LHC, all trigger and readout electronics need to be replaced by new ones.

Thin Gap Chamber (TGC) for ATLAS

ATLAS detector   TGC

Φ (strip)
R (wire)
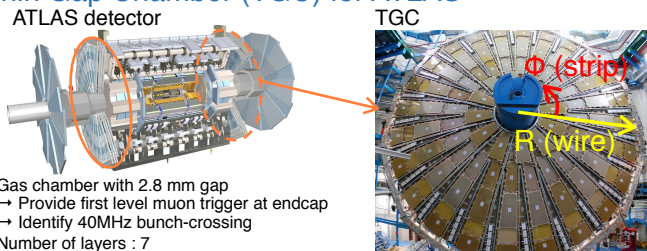
Gas chamber with 2.8 mm gap
→ Provide first level muon trigger at endcap
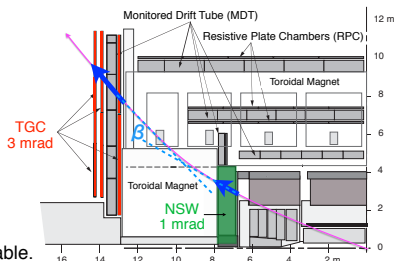→ Identify 40MHz bunch-crossing
Number of layers : 7

TGC Track Trigger

1. Trigger Algorithm

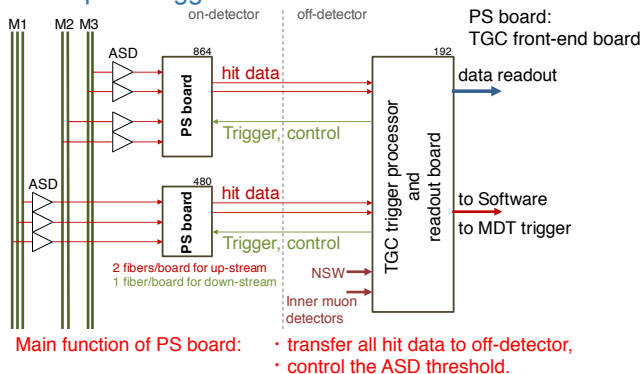Current TGC trigger:
  coincidence-based trigger

TGC trigger for HL-LHC:
  track-based trigger
  (Trigger decision: β)

Before the start of HL-LHC,
NSW 1mrad measurement available.

Monitored Drift Tube (MDT)
Resistive Plate Chambers (RPC)
Toroidal Magnet
TGC 3 mrad
β
Toroidal Magnet
NSW 1 mrad

Momentum resolution at the trigger improved by TGC tracking. Rate for single muon trigger with p_T threshold of 15 GeV reduced by 30% in the endcaps.

2. Concept of Trigger and Readout Electronics

M1 M2 M3
on-detector   off-detector
ASD
864
PS board
hit data
Trigger, control
192
data readout
PS board:
TGC front-end board

ASD
480
PS board
hit data
Trigger, control
TGC trigger processor and readout board
to Software
to MDT trigger

2 fibers/board for up-stream
1 fiber/board for down-stream
NSW
Inner muon detectors

Main function of PS board:
· transfer all hit data to off-detector,
· control the ASD threshold.

Prototype of TGC PS Board

For the timing alignment
(old) Patch-Panel ASIC
4 on mother board
4 on daughter board
32 × 8 = 256 channels

This prototype board has all functions for HL-LHC!

For hit data transfer and control of Patch-Panel ASIC and DAC
FPGA
Xilinx Kintex-7
XC7K325TFFG900-2
256 channel data Tx
PP ASIC control via JTAG
DAC control via I²C

Optical Rx/Tx
2 Tx and 2 Rx
(up to 20 Gbps)

Ethernet
for debugging

TTC

For ASD threshold supply and monitoring
DAC
DAC7578SPW
8 channels × 2
ADC
LTC1289CCSW
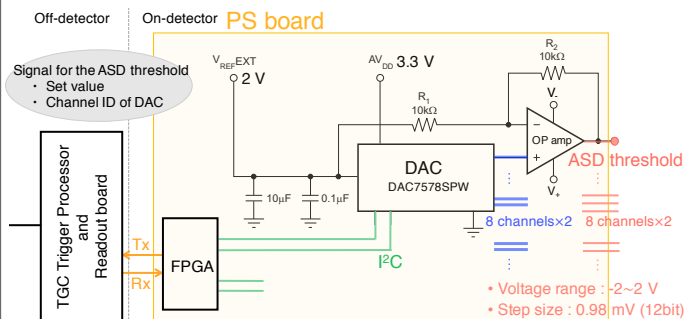
Performance Test

1. Demonstration of the Data Transfer

Measure the bit error rate with loop back by a transceiver for high-speed data transfer by Xilinx's IBERT.
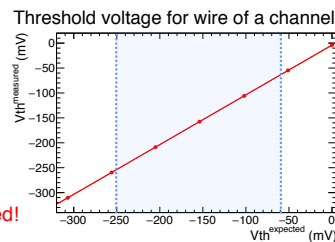
Eye Diagram from IBERT
Voltage offset
Bit error rate
Unit interval

Data transfer rate
8.0 Gbps × 2

Bit error rate < 8.91×10⁻¹⁵
Data transfer of 16 Gbps has been successfully demonstrated!
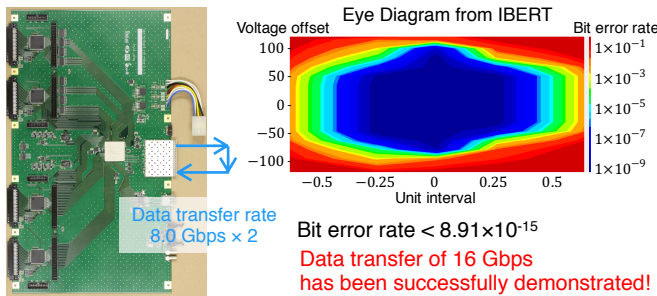
2. Demonstration of the ASD Threshold Control

Off-detector   On-detector   PS board

Signal for the ASD threshold
· Set value
· Channel ID of DAC

V_{REF}EXT 2 V
AV_{DD} 3.3 V
R_2 10kΩ
R_1 10kΩ
OP amp
V_-
V_+
ASD threshold
DAC DAC7578SPW
10μF   0.1μF
8 channels×2   8 channels×2
I²C

TGC Trigger Processor and Readout board
FPGA
Tx
Rx

· Voltage range : -2~2 V
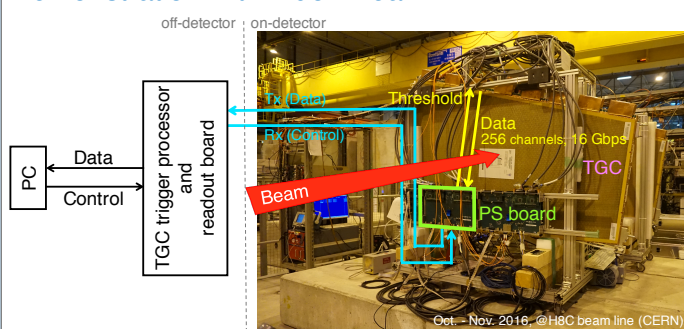· Step size : 0.98 mV (12bit)

Measure the ASD threshold with digital voltmeter.

Range of the value in Run-2 operation
  Wire : -250 mV~60 mV
  Strip : 70 mV~160 mV

Perfect linearity between the set and the measured values are obtained!

Threshold voltage for wire of a channel
$Vth^{measured}$ (mV)
$Vth^{expected}$ (mV)

Demonstration with Muon Beam

off-detector | on-detector
PC
Data
Control
TGC trigger processor and readout board
Tx (Data)
Rx (Control)
Threshold
Data 256 channels; 16 Gbps
Beam
TGC
PS board
Oct. – Nov. 2016 @H8C beam line (CERN)

Efficiency for a channel has been estimated from the events which have one hit for each layer other than the layer of interest.

· Most of the channels in the beam area has almost 100% efficiency.
· The efficiency is relatively small for some channels.
  →Due to support structure of the wires inside the chamber.

Wire support
Button support
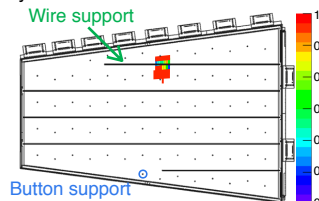
Basic functionalities of the TGC PS board have been demonstrated!

Conclusion

· A prototype of PS board has been developed with the concept for HL-LHC,
  - all hit data transfer with 16 Gbps per board,
  - ASD threshold control and monitoring based on FPGA.
· The prototype of PS board has been successfully demonstrated.