Recent developments of the silicon detector

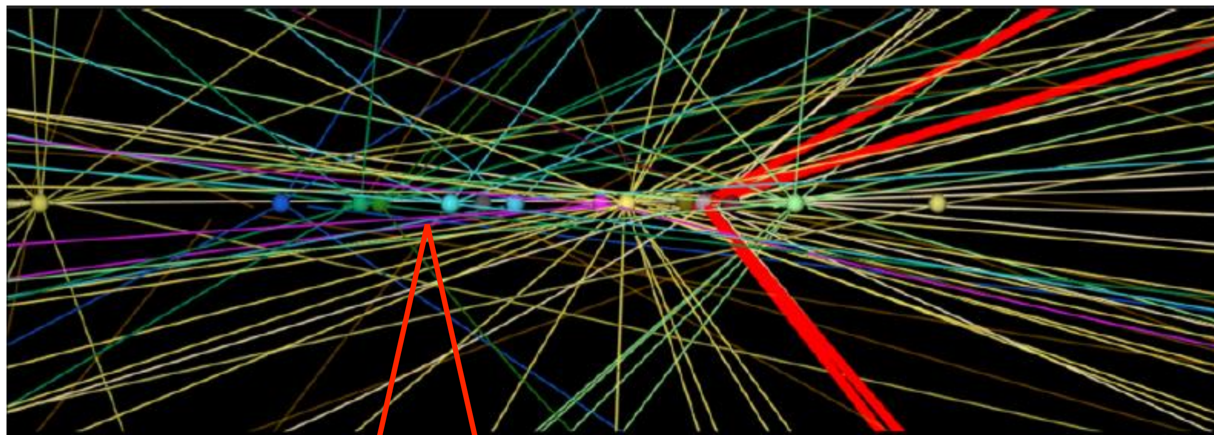
将来計画委員会勉強会 『測定器開発フロンティア勉強会』

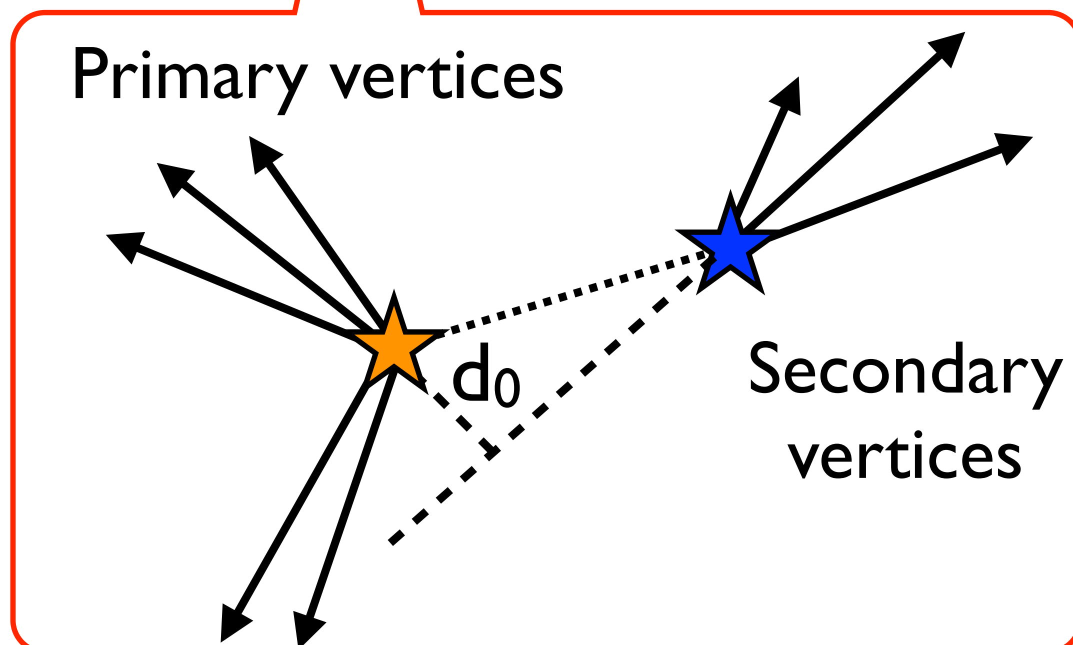
2021/08/27

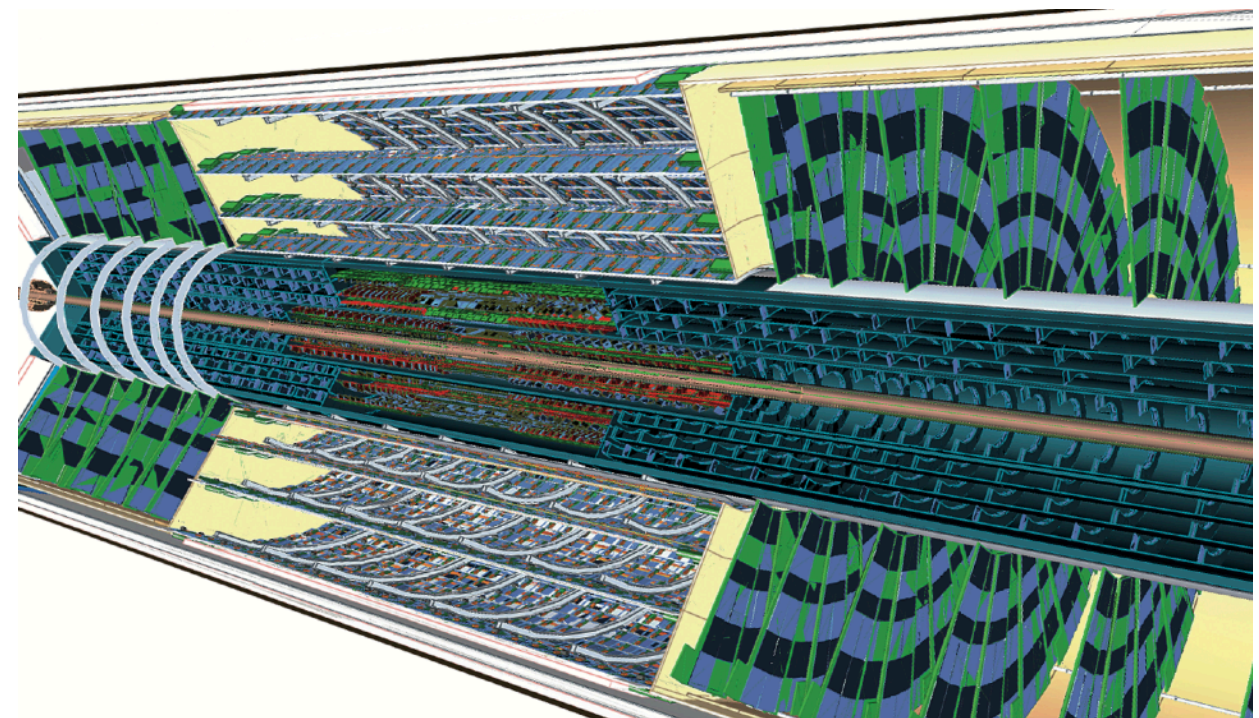
KEK, IPNS,
Manabu Togawa

Silicon detector for collider experiments

- Silicon tracker play an impotent role for recent collider experiment
  - Long life particle tagging by looking at the displacement.
  - Find vertex point. -> Separation of vertex points.



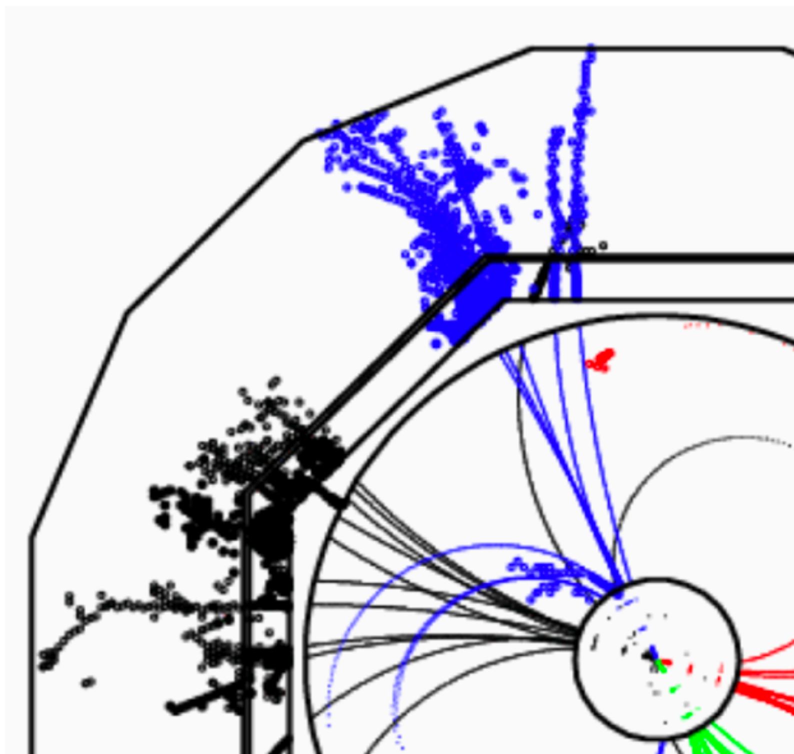




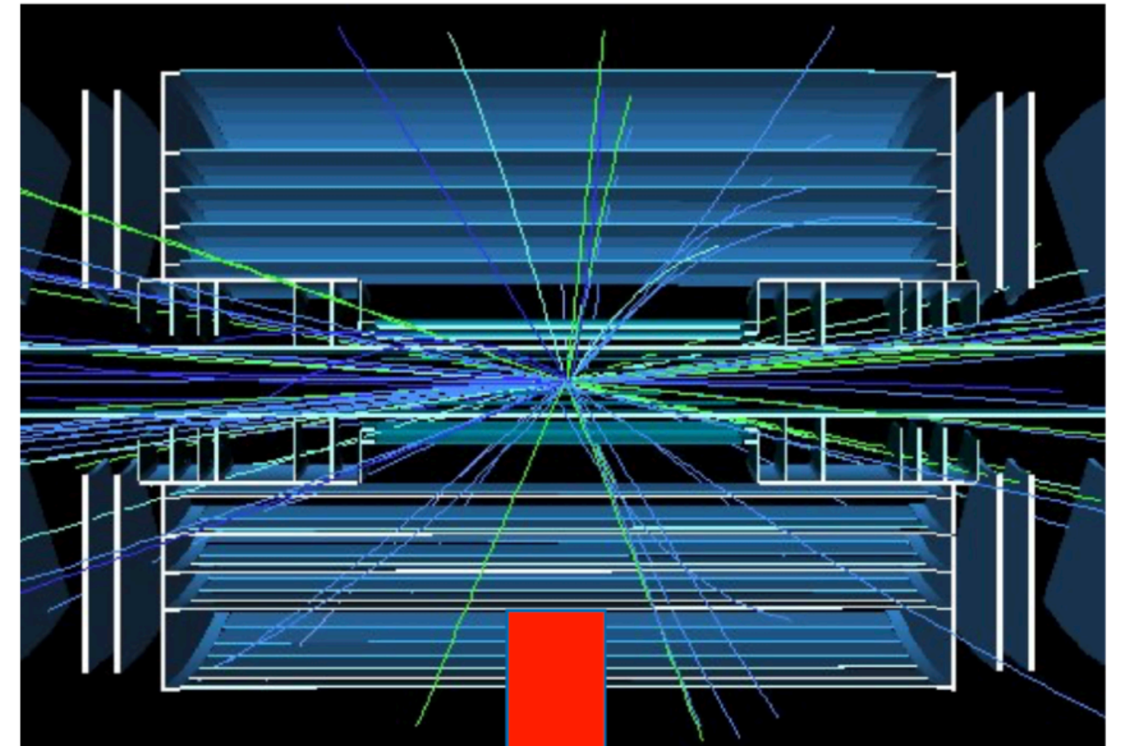
ATLAS ITk for HL-HLC

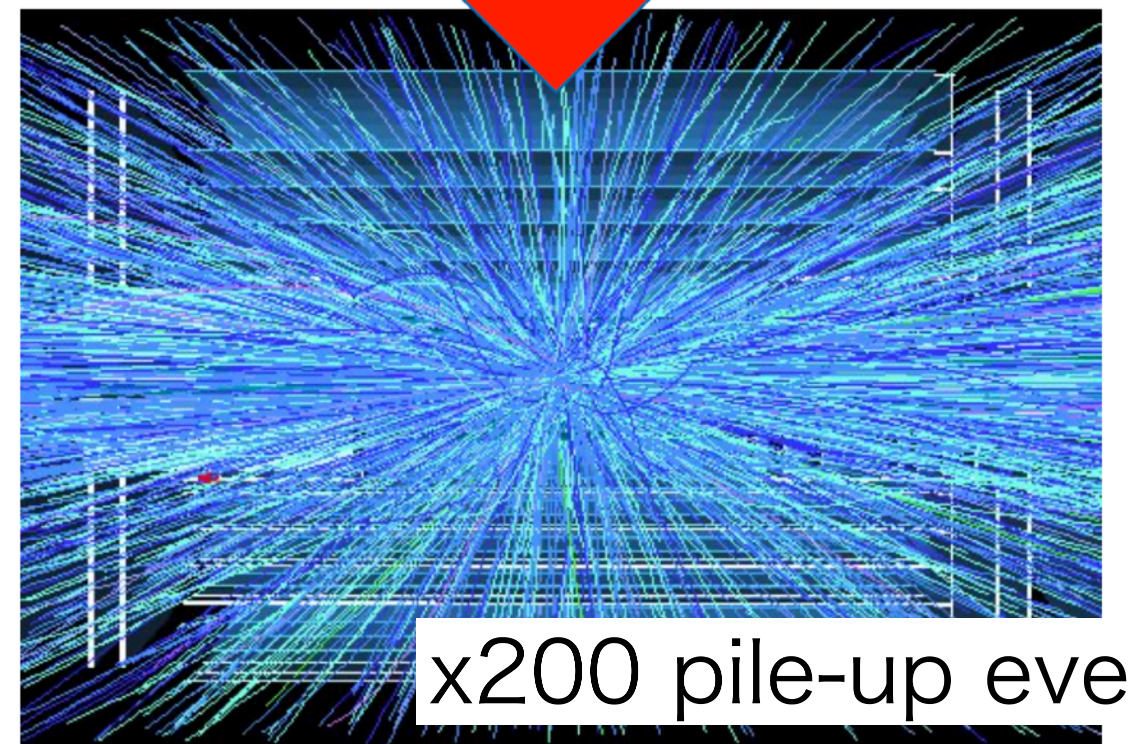
The experimental challenges

- Very high luminosity environment.
  - Not only vertex separation, but also radiation hardness.
- More precise measurement
  - Particle Flow Calorimetry



Particle Flow Calorimetry (ILC)





x200 pile-up events

Pile-up event (LHC)

The experimental challenges

	High luminosity		High precision
	pp (e.g. HL-LHC)		e^+e^- (e.g. ILC)
pile-up	10-20 um (50x50 pixels)	Spacial resolution	Few um
	few 10 ps	Timing	few 10 ps
		Material budget	< 0.1%
	10 MGy	Radiation hardness	

Data rate, Low power

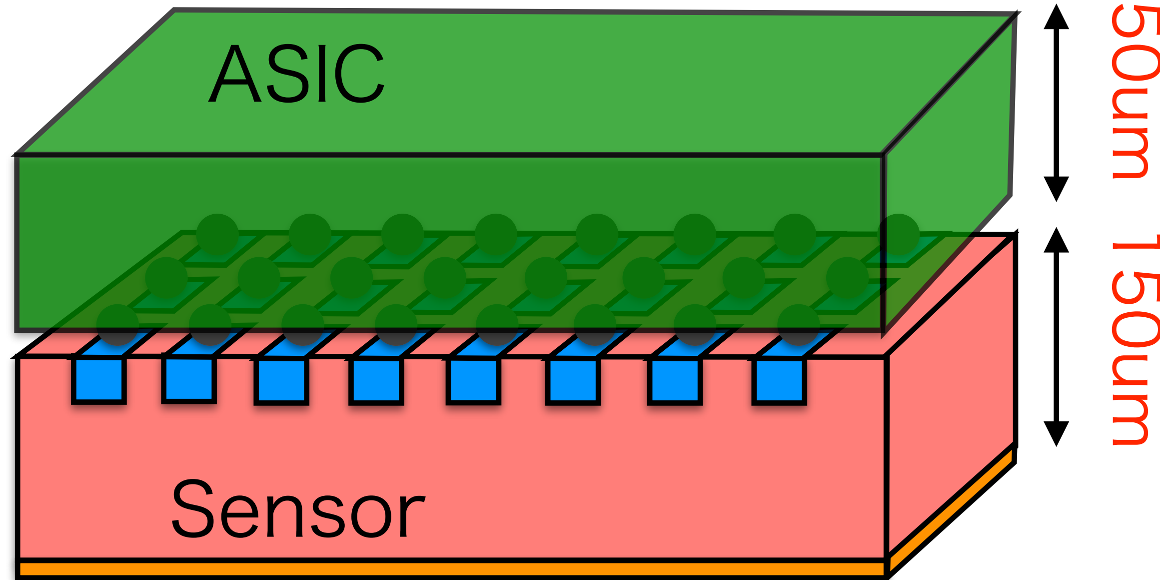
- ASIC, Links, Mechanics, Software are also important.

Silicon sensor type

Hybrid

Planer | 3D

65 nm LSI process

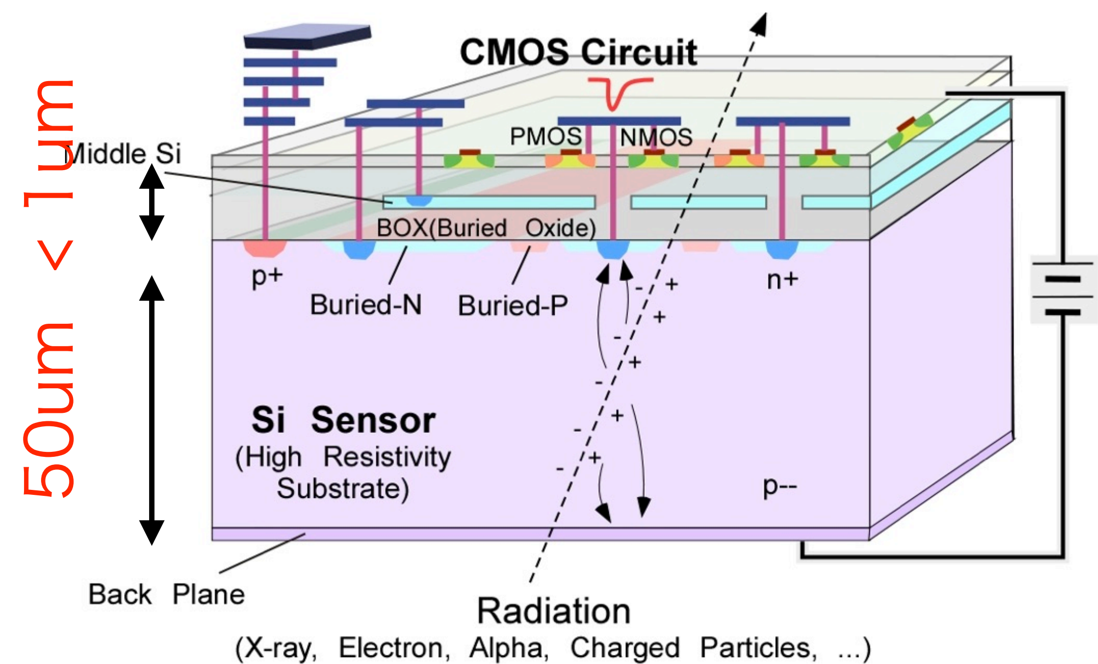


- Sensor and ASIC can be designed and processed separately.
- Well separation btw Sensor and ASIC, No cross talk.
- Bump bonding limits pixel size and total thickness

Monolithic

SOI | CMOS

200 nm LSI process | 180 nm LSI process



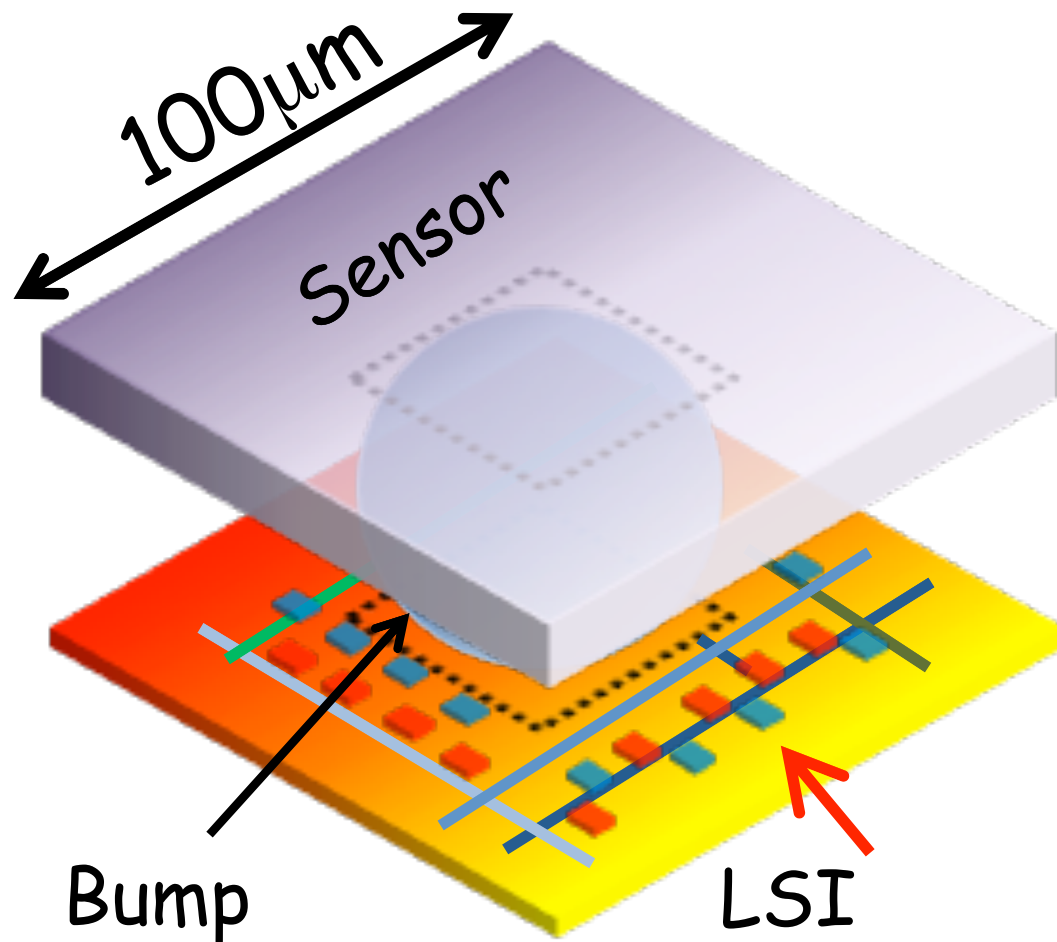
- In principle, everything is better since circuit is direct connected to sensor
  - Low noise, high speed, Low power
  - Low cost (No bonding process)
  - Small pixel size, Thinner

Material budget

- Only few vender have processed.

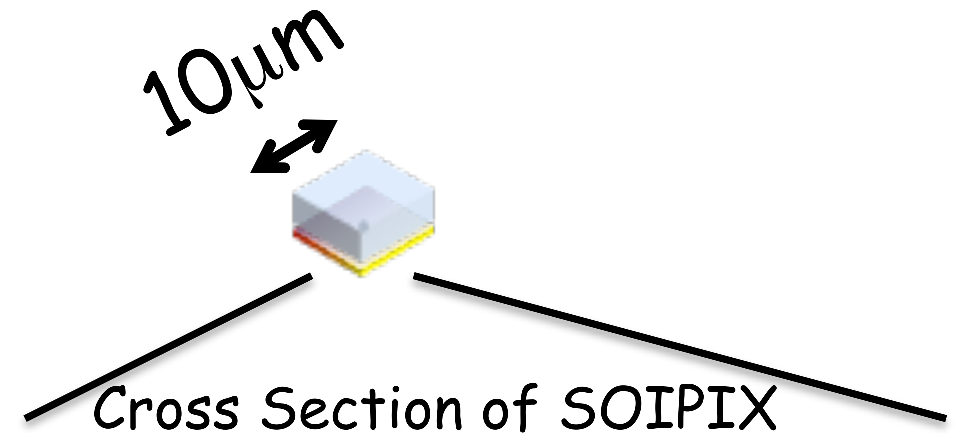
Pixel size limitation

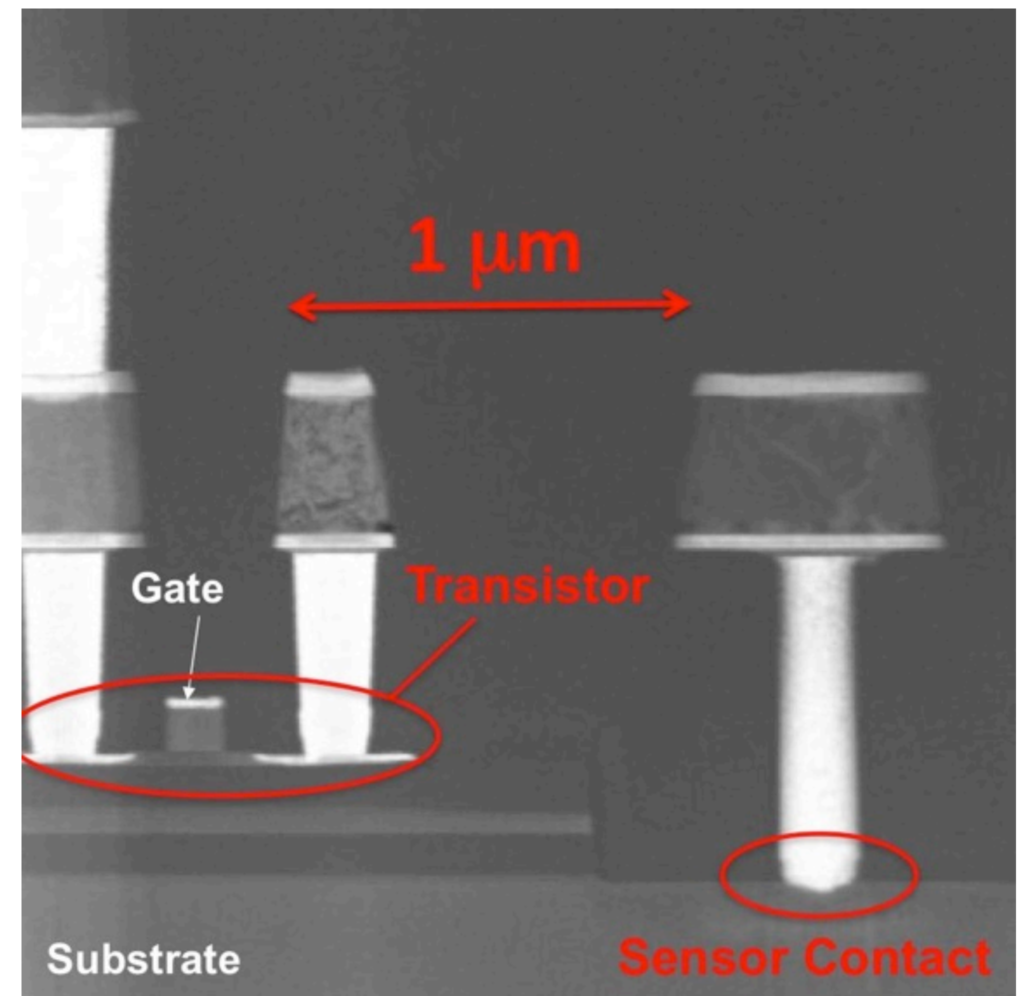
Hybrid



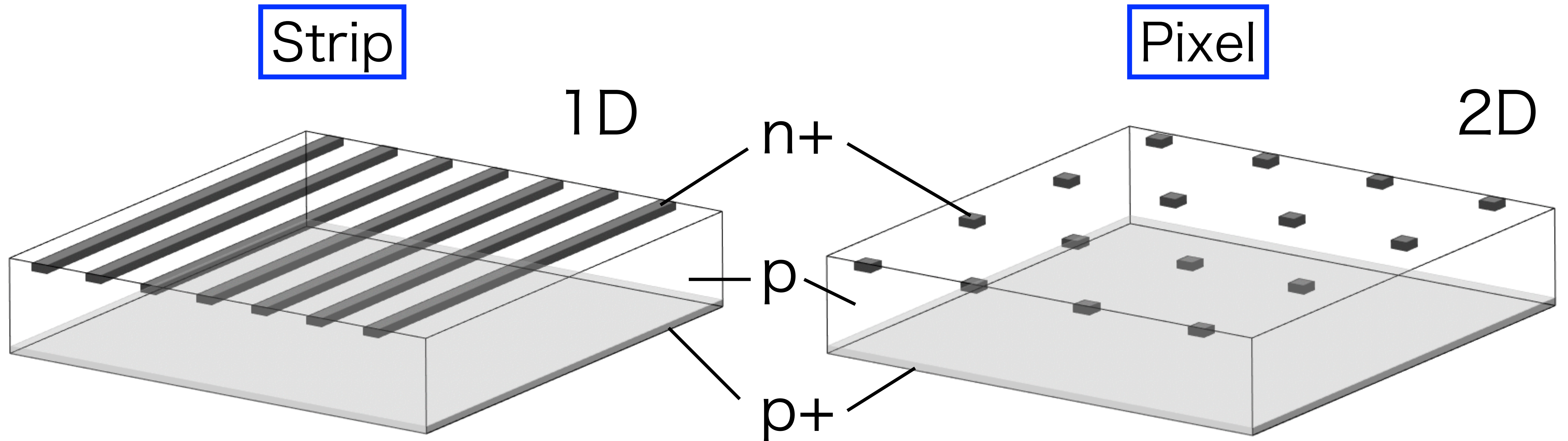
- Bump size ~ 20 µm for 50x50 µm pixel
  - Already expensive..
- Monolithic can be small within the process rule.

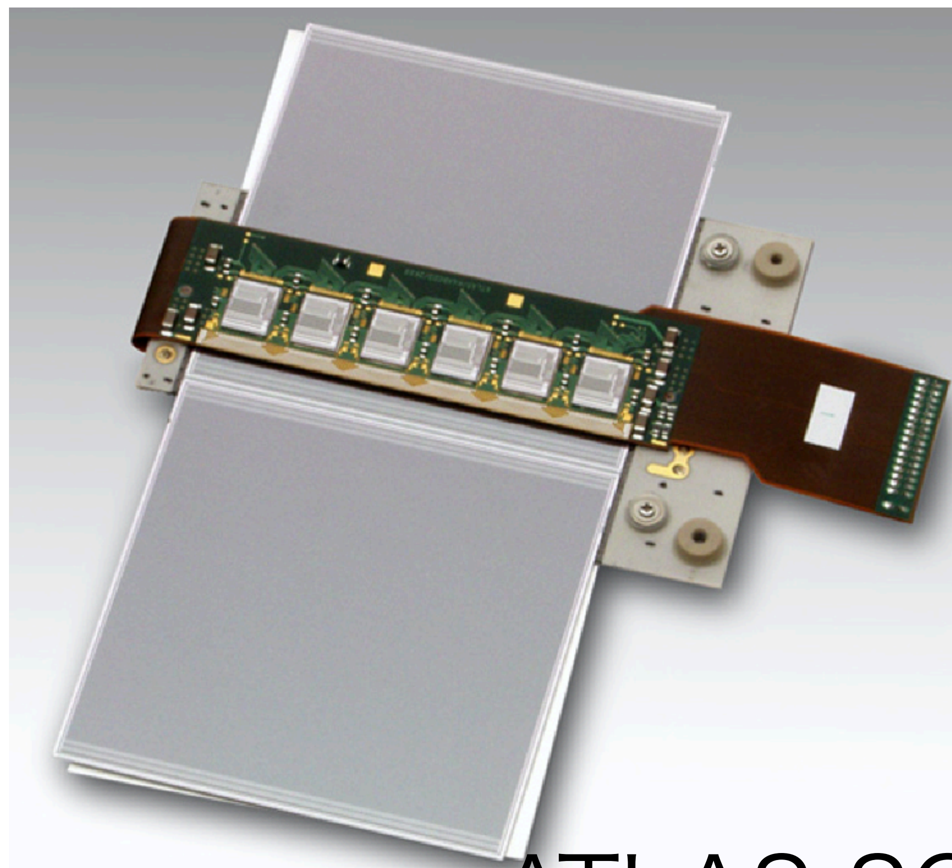
Monolithic





Planar sensor



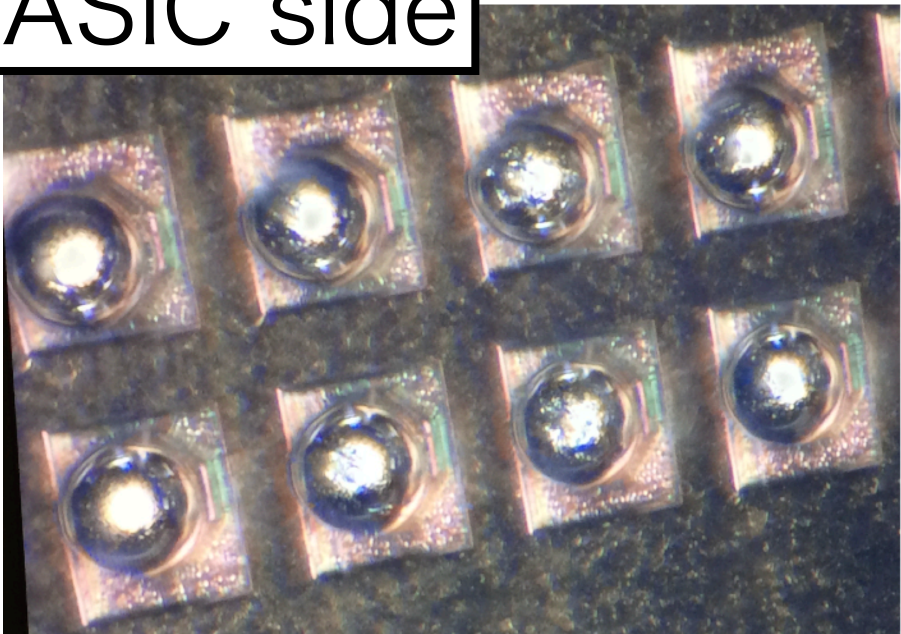


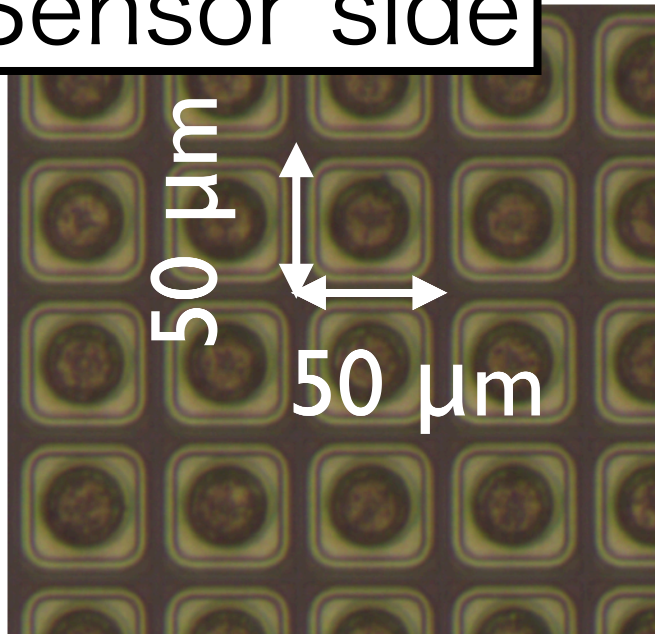
ATLAS SCT

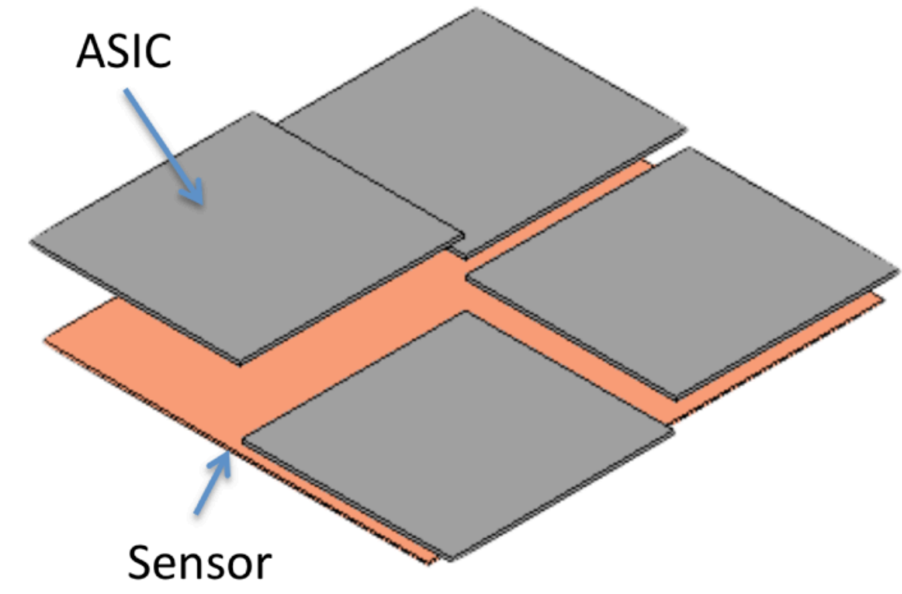
- “Traditional type” silicon sensor
  - Depletion layer is increasing with bias voltage in thickness direction.
- This talk mainly focused on the pixel type.

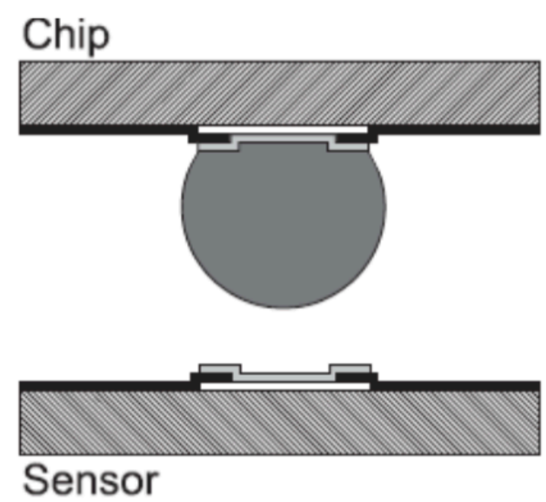
Hybrid

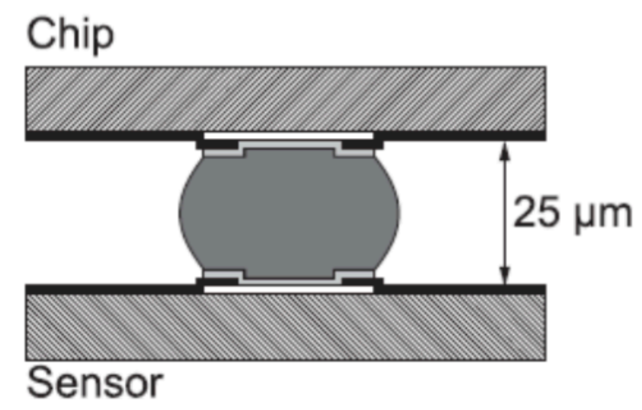
Planner sensor
Hybrid (Sensor + ASIC) : ATLAS pixel



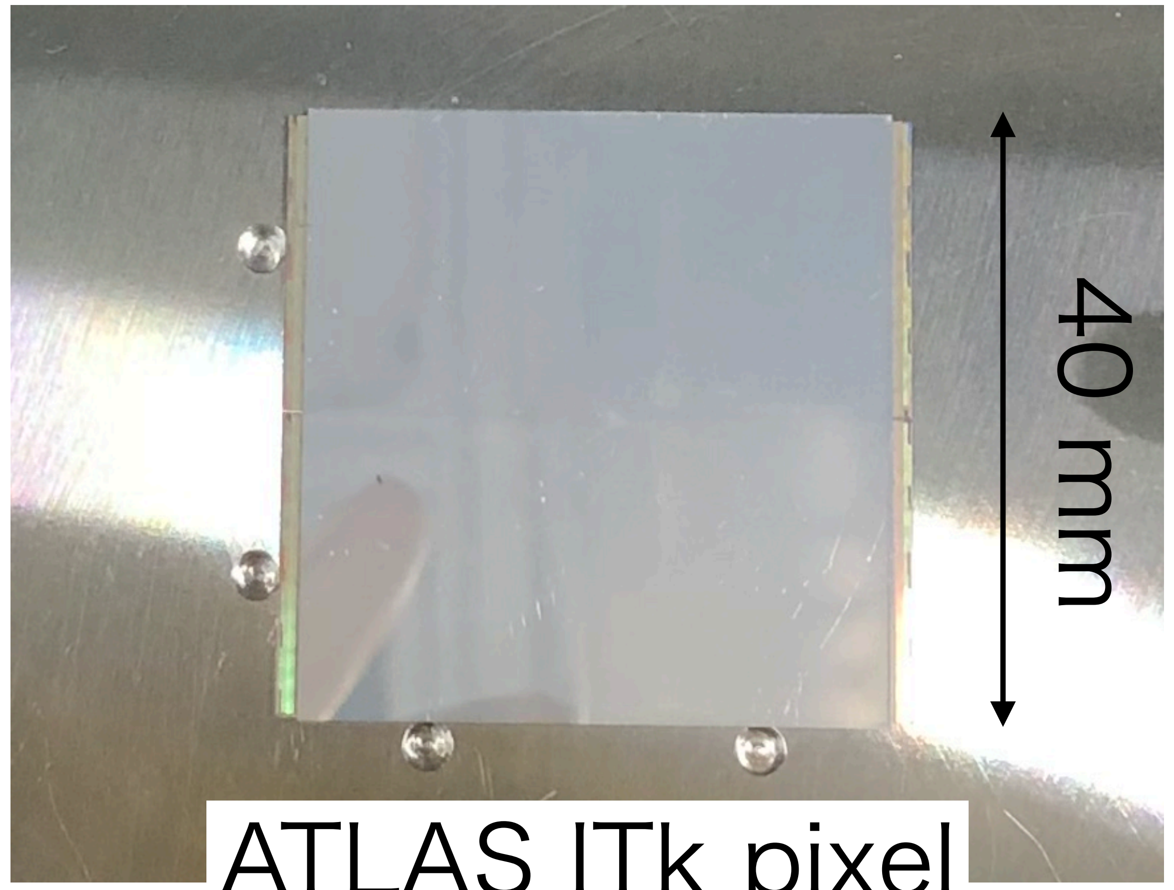




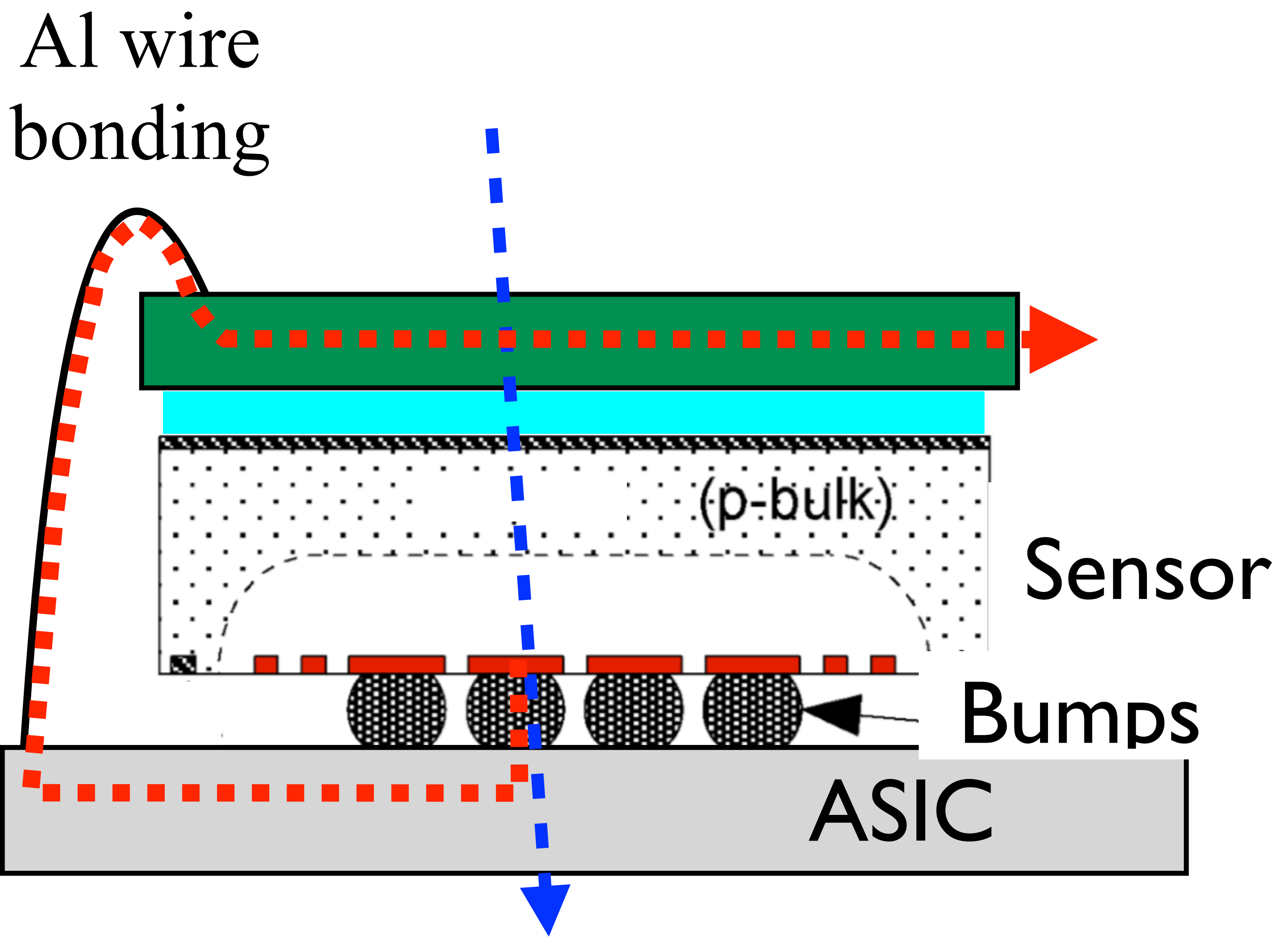


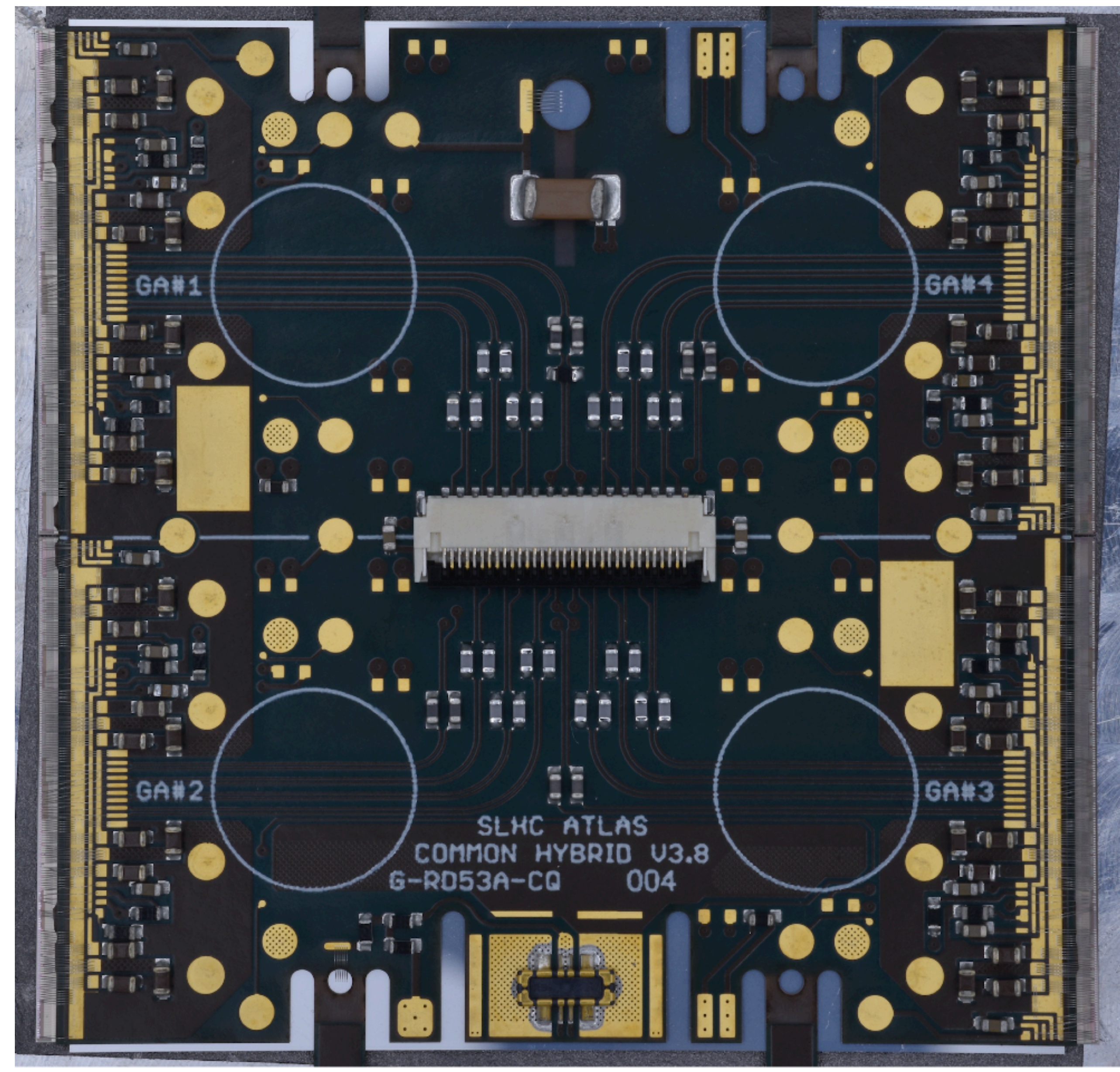


- Connection each pixels by metal bumps



Planner sensor
Hybrid (Sensor + ASIC) : ATLAS pixel

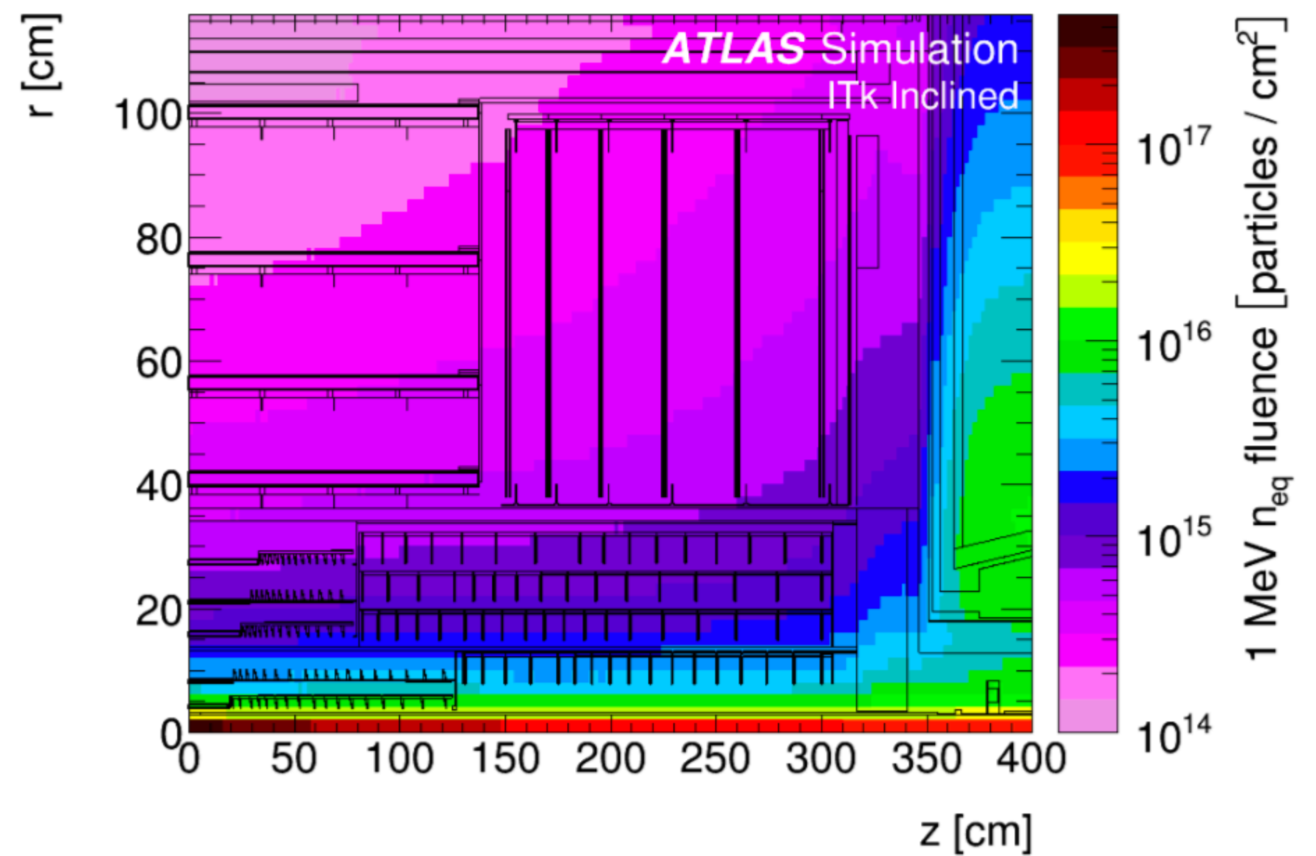


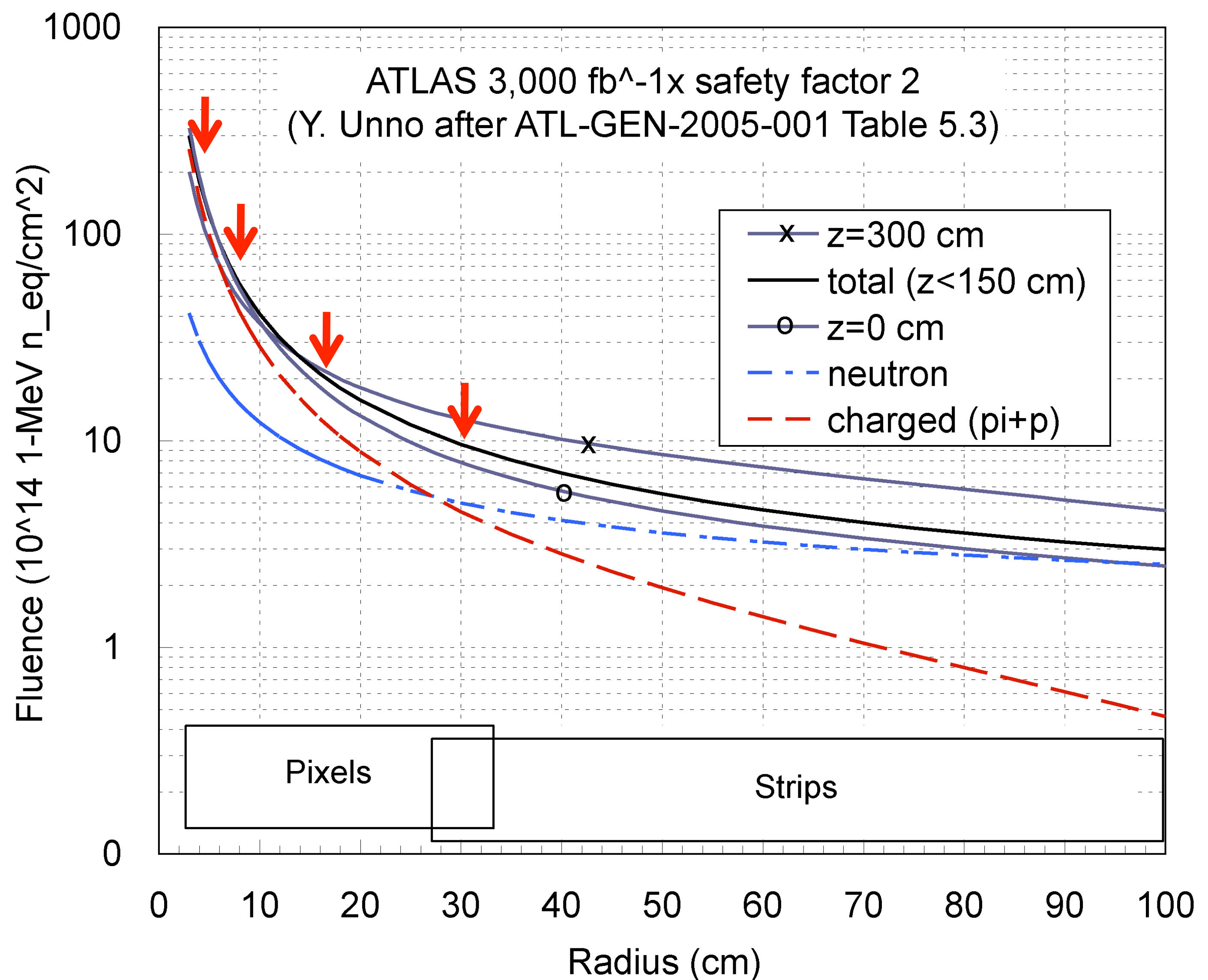


Radiation hardness

Radiation hardness Requirement for HL-LHC

- Instantaneous luminosity
  - $5\sim7\times10^{34}$ /cm^{-2}s^{-1}
    - ~200 events / crossing
- Rad. damage (1 MeV $n_{eq.}$/cm^2) :
  - Inner : r=3.7 cm : ~ 2×10^{16}
  - Mid. : r=7.5 cm : ~ 6×10^{15}
  - Outer : r=31 cm : ~ 1×10^{15}
- 1×10^{16} (1 MeV $n_{eq.}$/cm^2)
  - TID ~ 7 MGy @ pp collision





Radiation hardness

◉ 高放射線耐性，n-in-nより安い

⇐ 日本グループが推進

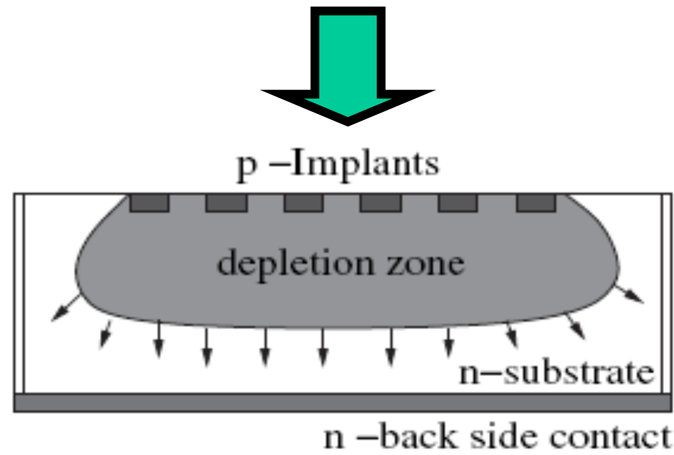
Radiation damage on sensor : Bulk damage

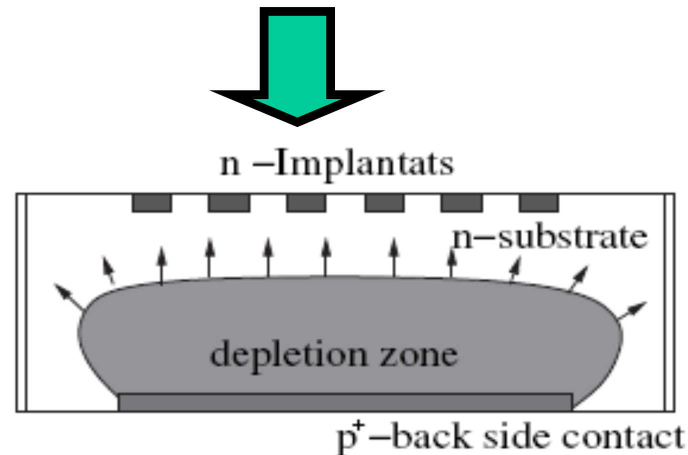
SCT

Pixel, IBL

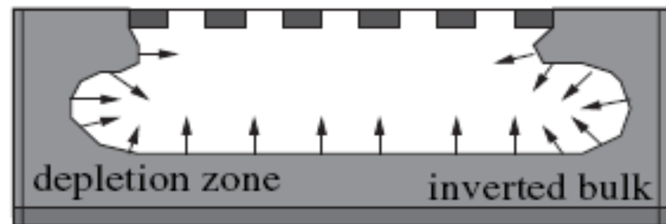
p⁺ in n "normal"

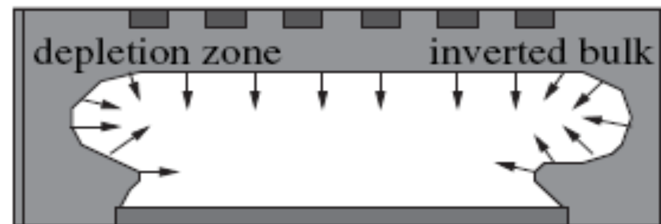
n⁺ in n





before type inversion





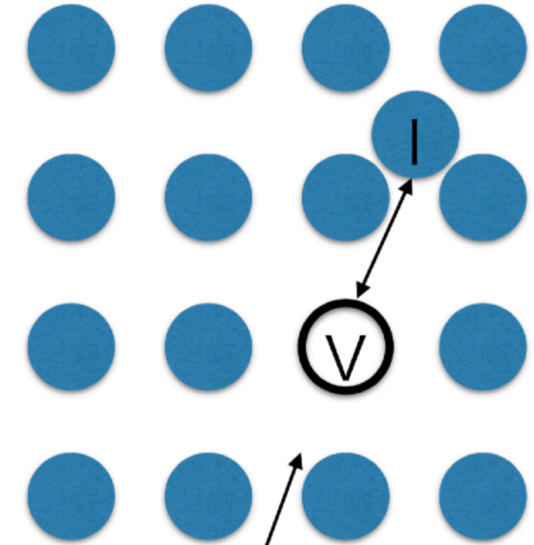
after type inversion

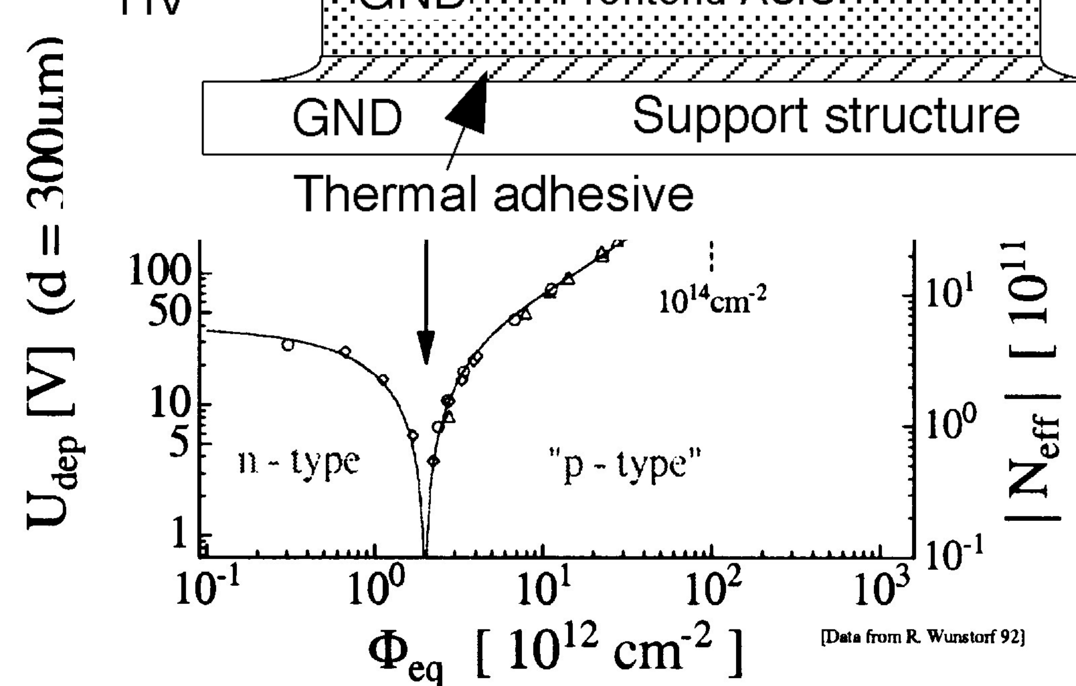
depleted inverted bulk

(f)

depleted inverted bulk

substrate.





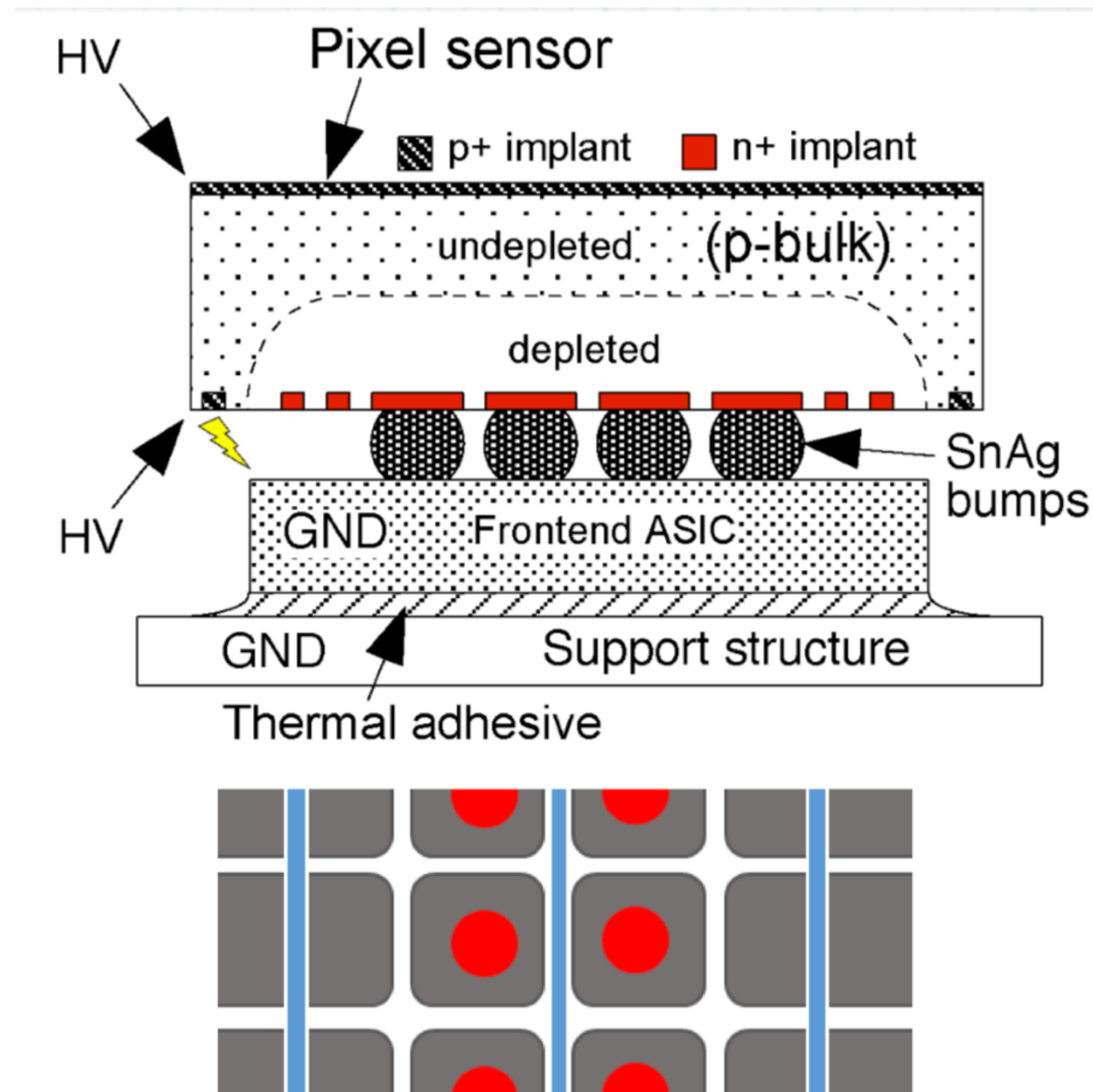
Radiation hardness

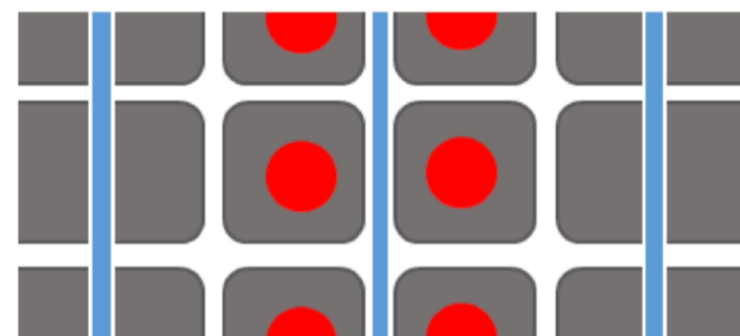
Hybrid

Silicon detector toward the HL-LHC

Sensor

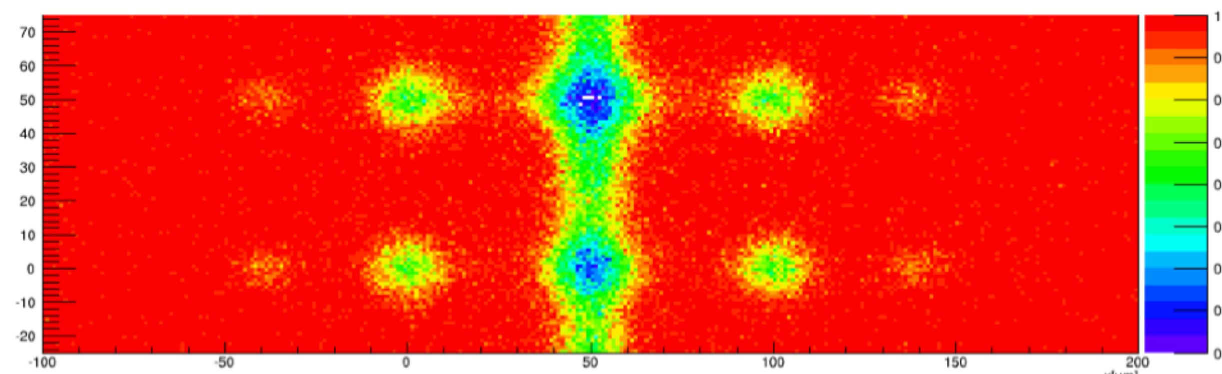
- n-in-p type：No type inversion
  - Full depletion has been raised due to the increasing of charge carrier.
    - ~600 V for 150 um thick planer @ 5×10^{15} (1 MeV $n_{eq.}/cm^2$)
  - Charge collection efficiency has been reduced due to the defect increasing





ASIC

- New Circuit design (RD53 group)
  - Redundant circuit to prevent SEE
  - Low noise to keep efficiency

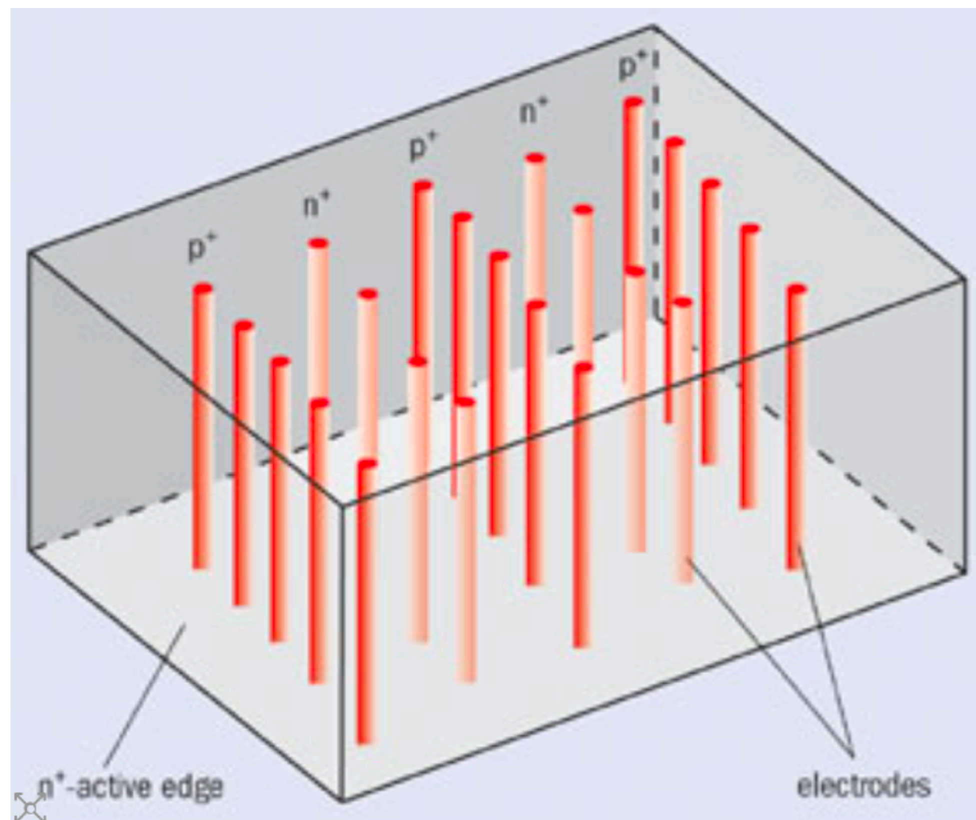


Low efficiency at border of pixels. -> Solved

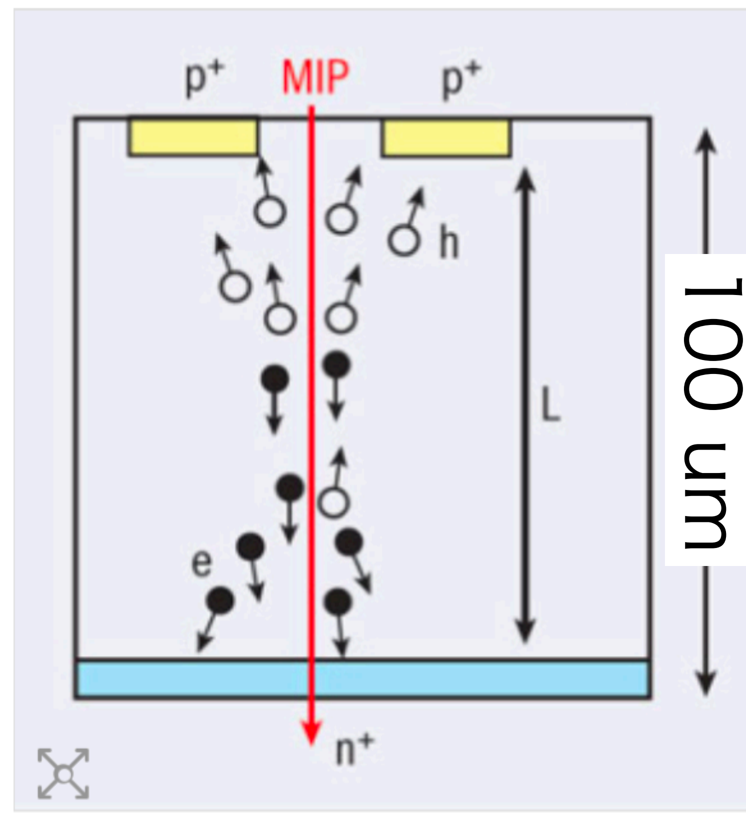
Hybrid

3D sensor

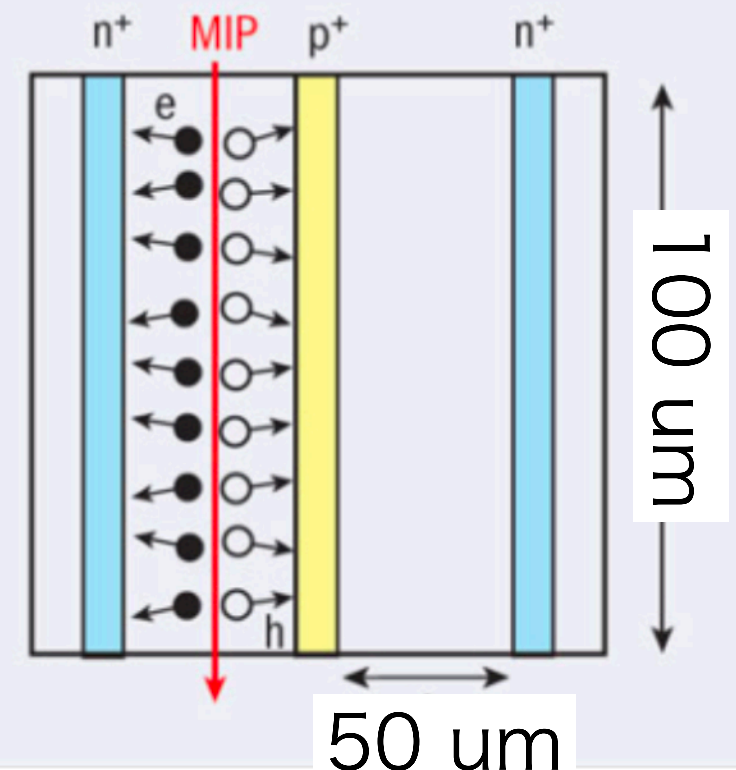
3D structure



Planer



3D



Values are in case of ATLAS inner pixel

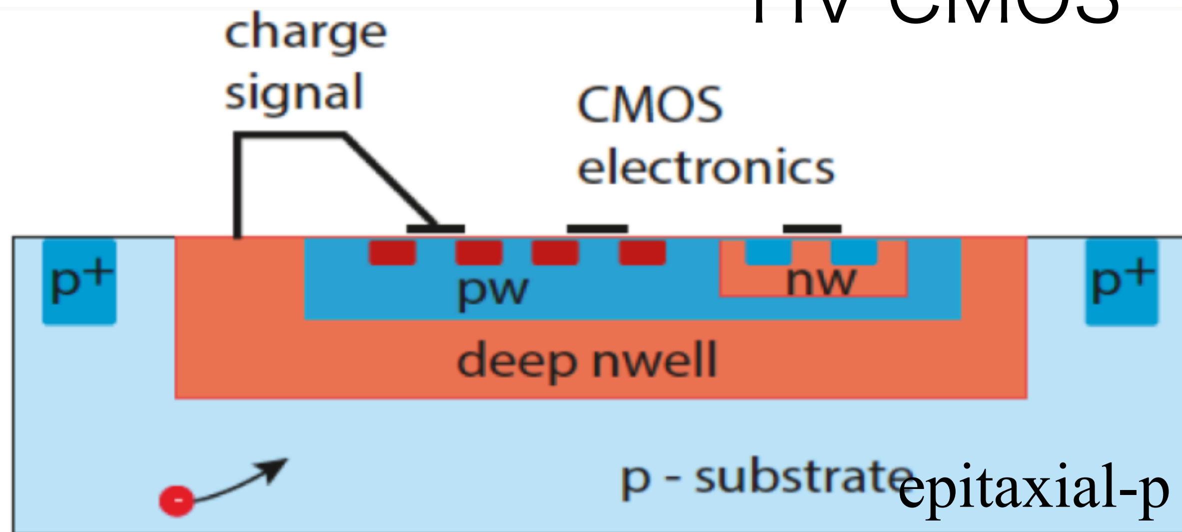
- In case of 100 um thick sensor,
  - Drift length is determined by the electrode pitch, 50 um
    - Depletion length ∝ sqrt(V) -> V reduces 1/4 than that of planer.
      - -> Operational with high radiation damage

Monolithic

CMOS sensor, two type

LFoundry 150 nm
AMS 180 nm

"HV CMOS"

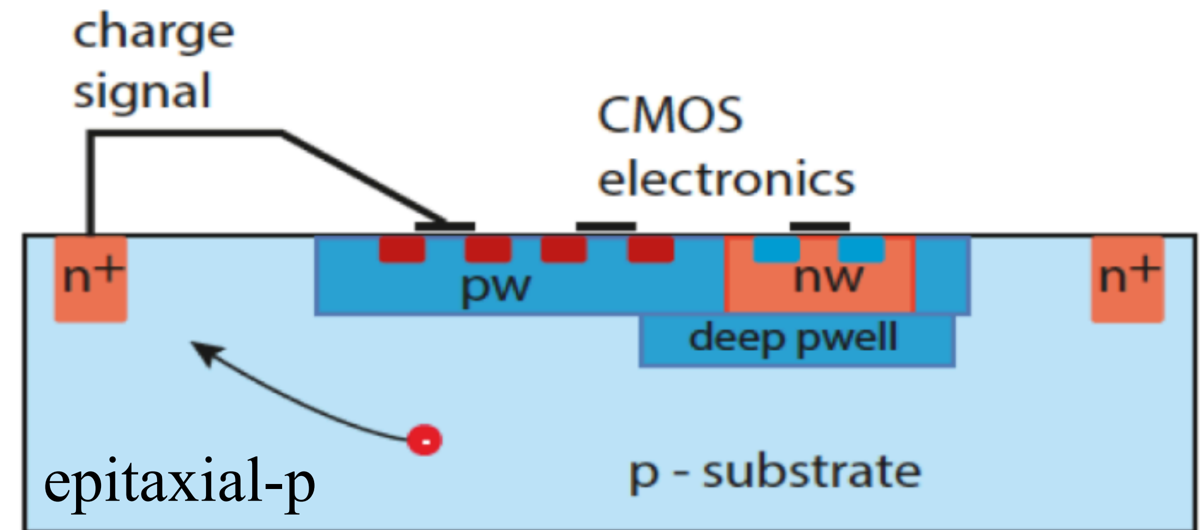


(a) Large fill-factor

- :) HV is possible
  - Uniform field, short drift distance
- :(Large inter well capacitance, Cpw (btw pw and deep nwell)
  - Bad noise, speed, power and cross talk…

Mu3e @ PSI

Tower Jazz 180 nm



(b) Small fill-factor

- :) Very small resistance
  - Good noise, speed, power
- :(Very small bias voltage
  - Small depletion area
  - Most of e/h are collected by diffusion.

STAR @ RHIC
ALICE @ LHC

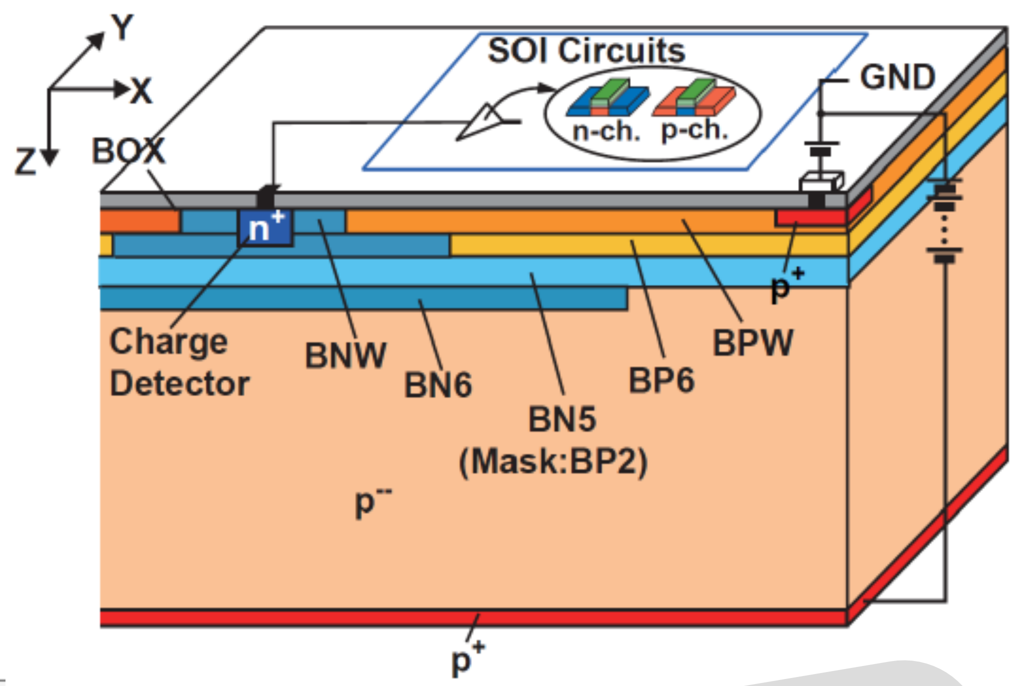
More details are summarized in Heinz's talk at https://kds.kek.jp/event/33154/

Monolithic

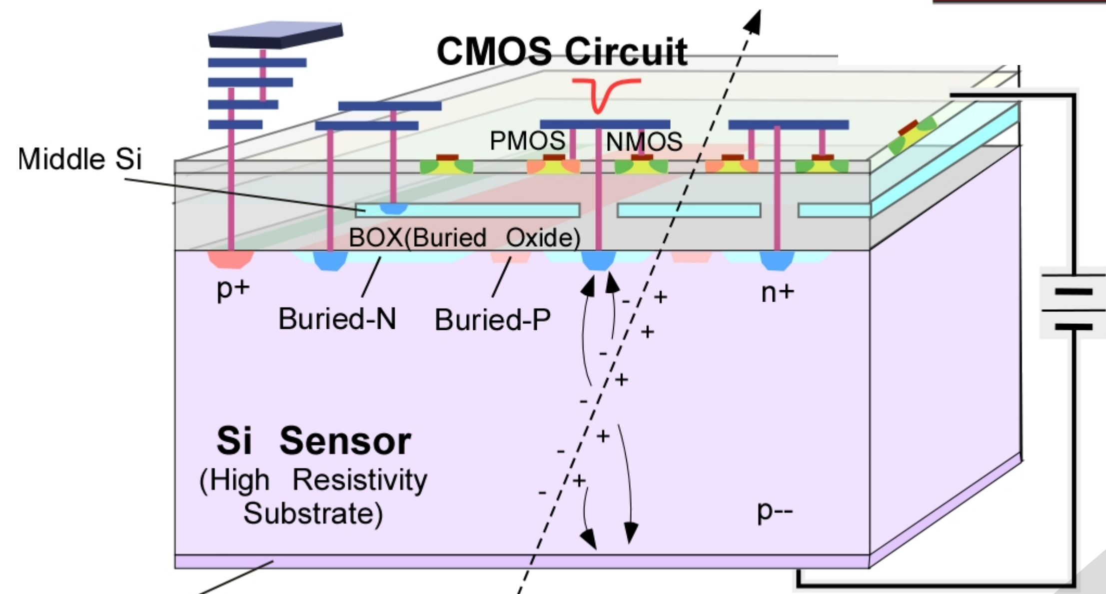
SOI
(Silicon On Insulator)

- Separation of circuit and sensor layers by insulator
- Optimize each layers ideally
  - high resistance on sensor and low on circuit

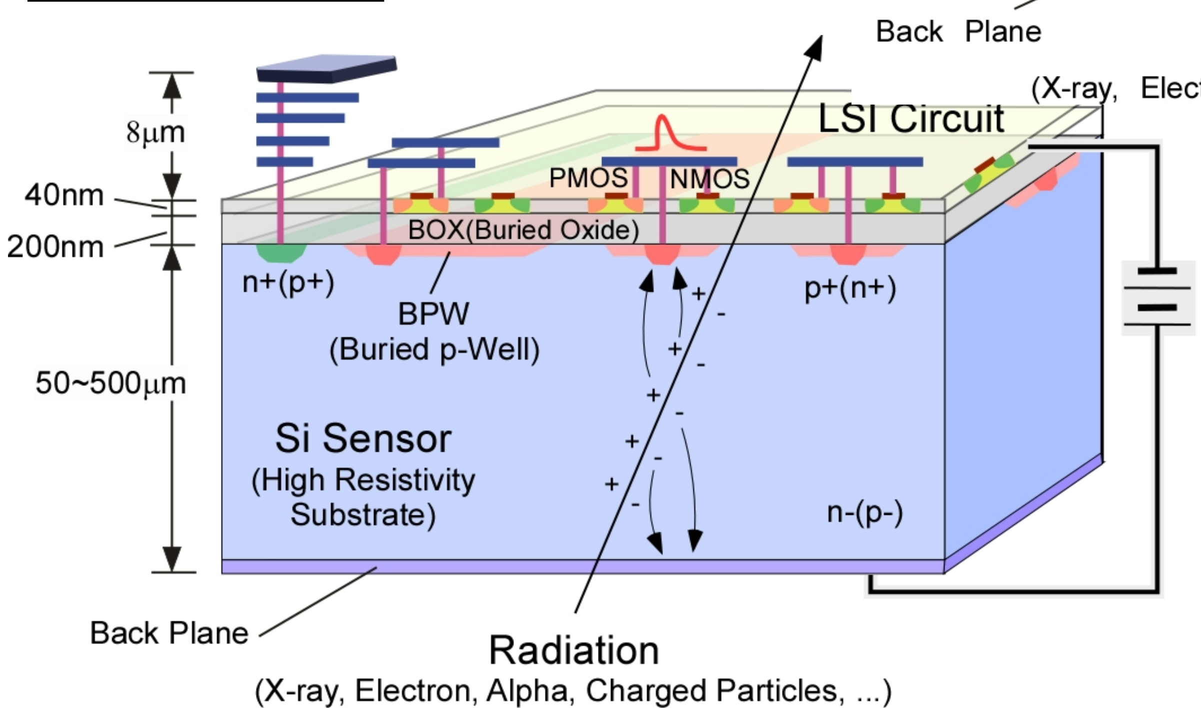
Single SOI with PDD



Double SOI



Single SOI

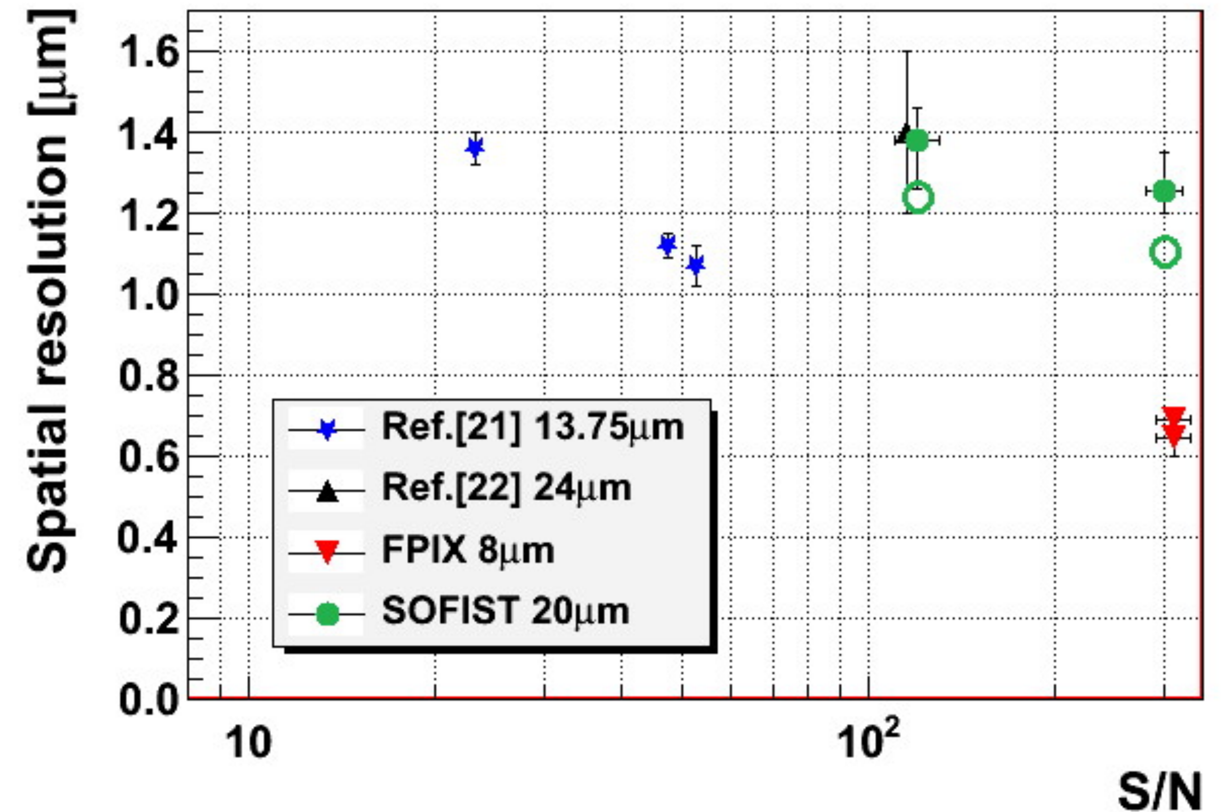


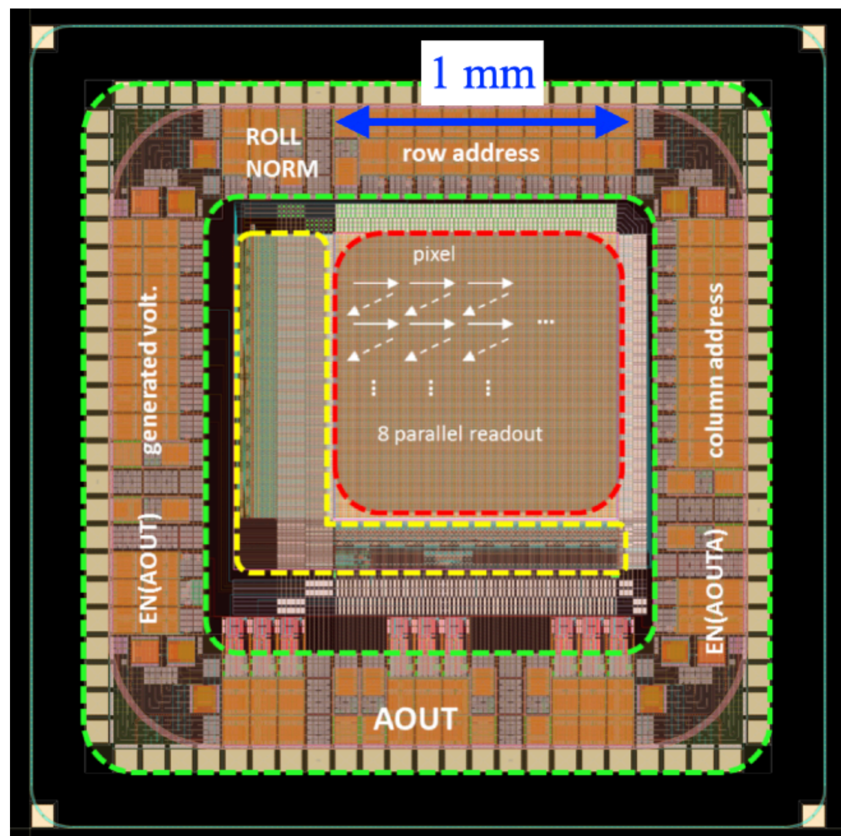
- Low capacitance
  - Good noise, speed, power
- HV can be supplied as planer
  - Normal p-n. Thick sensor can be applicable. <- X-ray application

Spatial resolution

Monolithic

- FPIX2 is the best record
  - 8 μm sq. pixels (128 x 128)
    - Sensitive area 1 mm sq.
  - Rolling shutter readout
    - 8 line parallel readout.
    - 1 ms frame time.





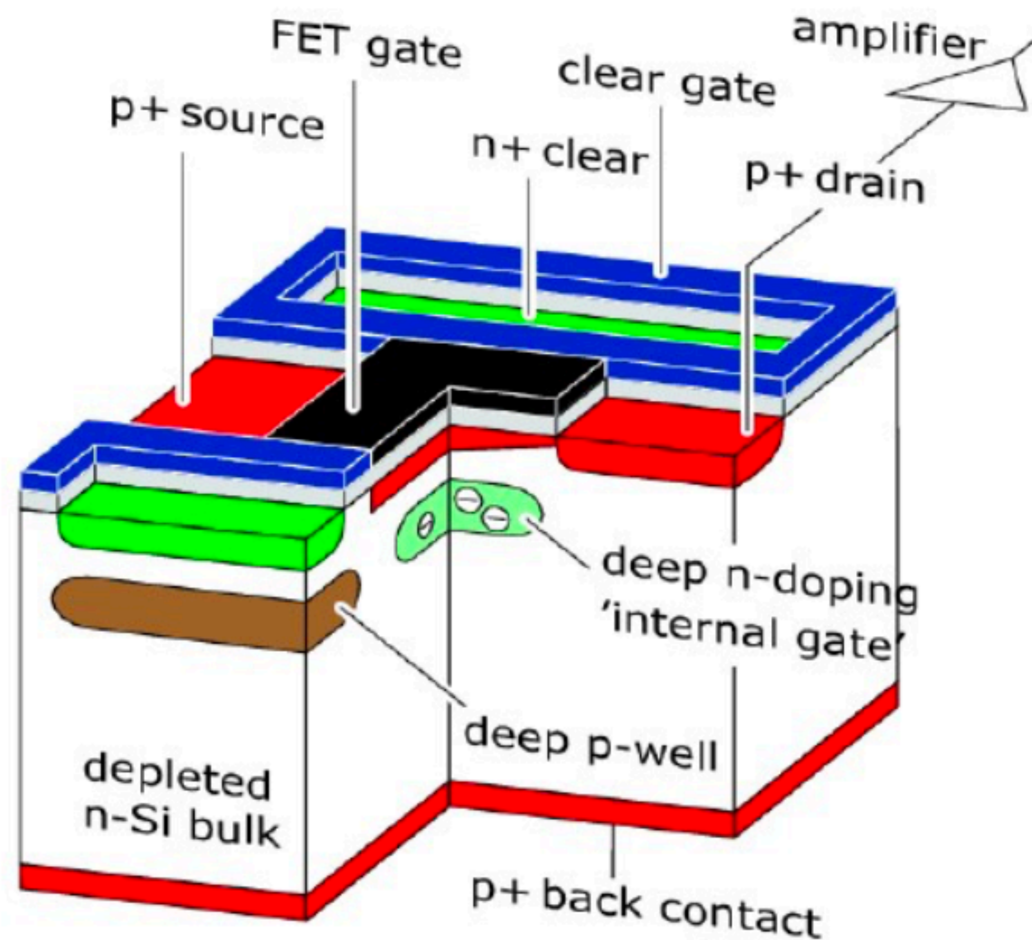
CMOS

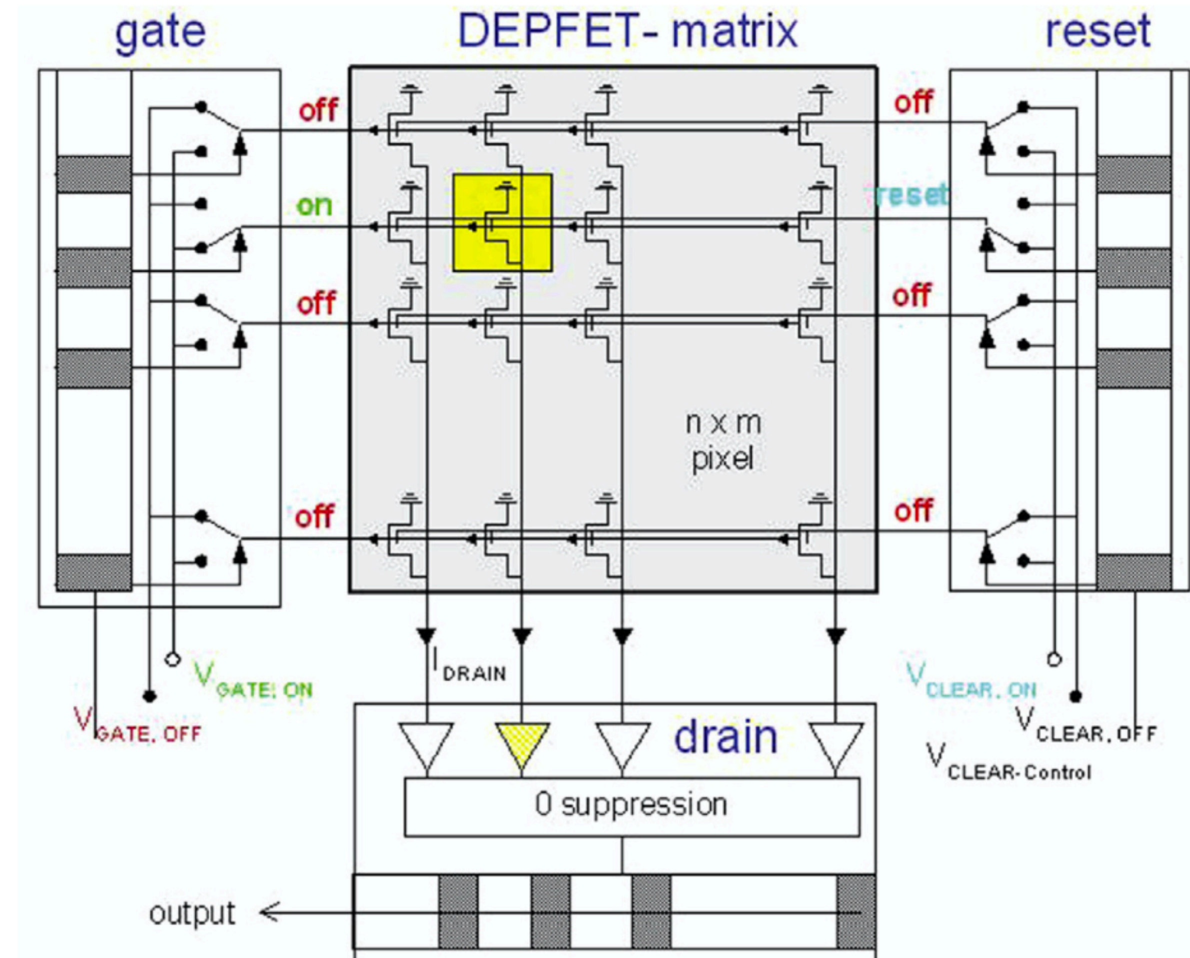
Detector	Pixel size	Resolution
ATLAS Pix	13.8 μm	1.1 μm
DEPFET	24 μm	1.4 μm
SOFIST	20 μm	**1.2 μm**
FPIX	8 μm	**0.65 μm**

PoS, Vetex2017 (2018) 035

DEPFET

NIM A 831 (2016) 85–87

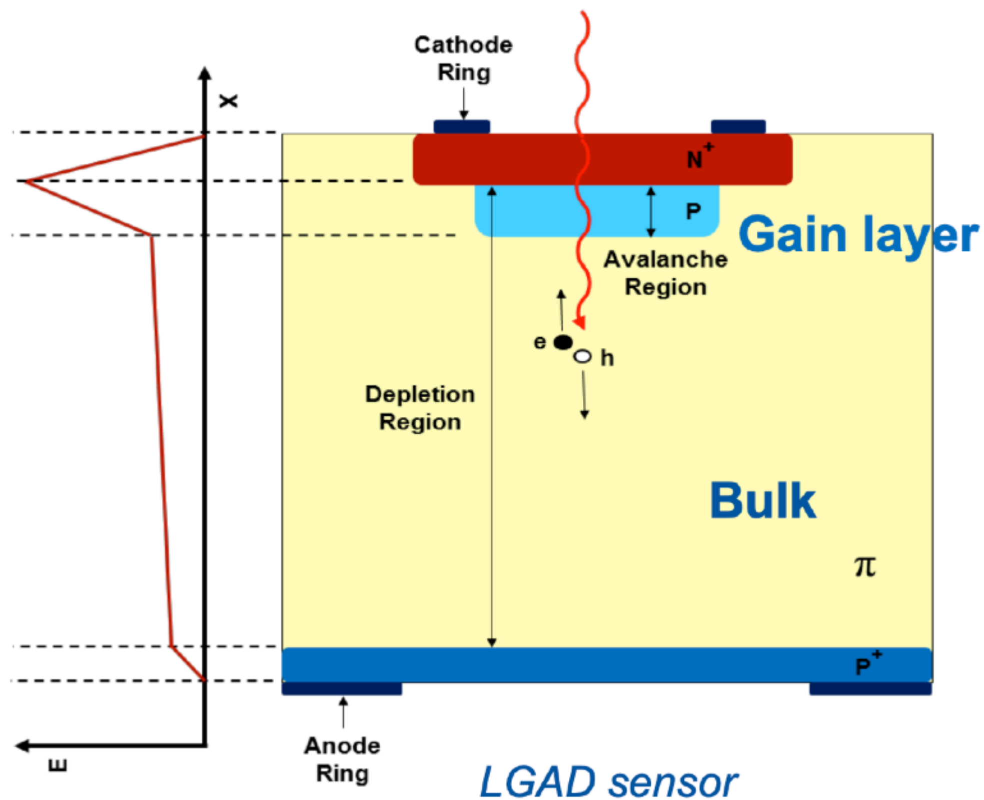


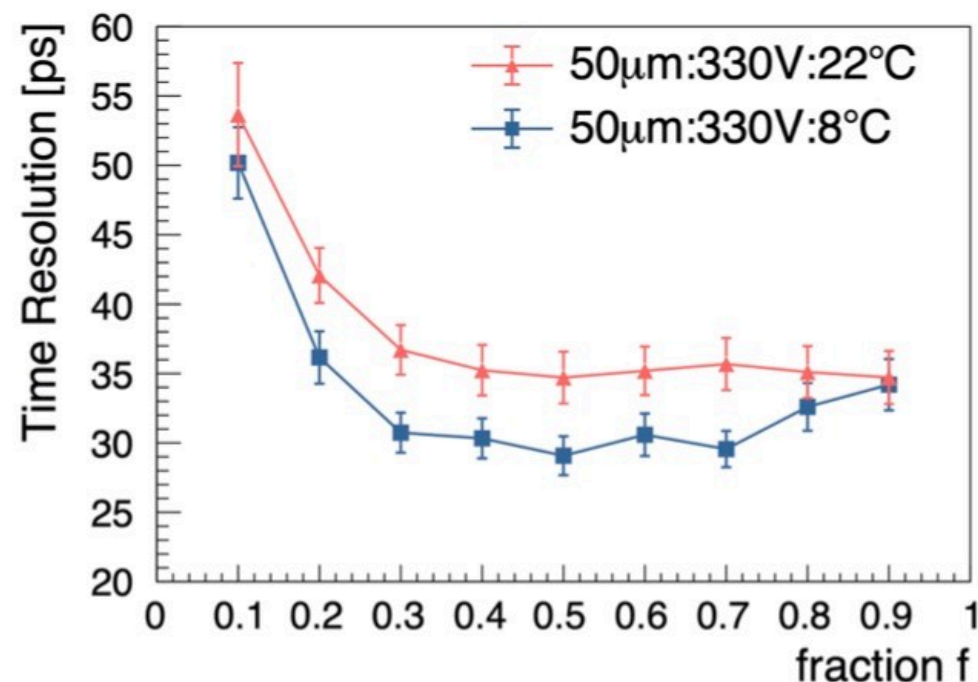


- DEPFET (Depleted p-channel FET)
  - Stored charge under the FET structure

Belle II

Timing resolution





LGAD

- Low Gain Avalanche Detector
- Multiply with low gain (~10) in thin gain layer
  - Fast rise time, Increase S/N
- Reached ~30 ps at few mm^2 size sensor
- Limitation :
  - Weighting field uniformity -> Favor large pixels
  - Radiation is OK up to 10^{15}

HGTD detector for HL-LHC (1.3x1.3 mm^2 pixel)

More detailed talk will be on RD platform workshop at 9/22 (Wed.) by Koji Nakamura https://kds.kek.jp/event/38615/

The experimental challenges toward the future

	High Energy		High precision
	pp (FCC/HE-LHC)		e^+e^- (e.g. ILC)
pile-up	5 um (20x20 pixels)	Spacial resolution	Few um
HLx10	few 10 ps	Timing	few 10 ps
		Material budget	< 0.1%
	100 MGy	Radiation hardness	

Data rate, Low power

- ASIC, Links, Mechanics, Software are also important.
- It is very challenging to go next generation of energy frontier.

KEK RD platform

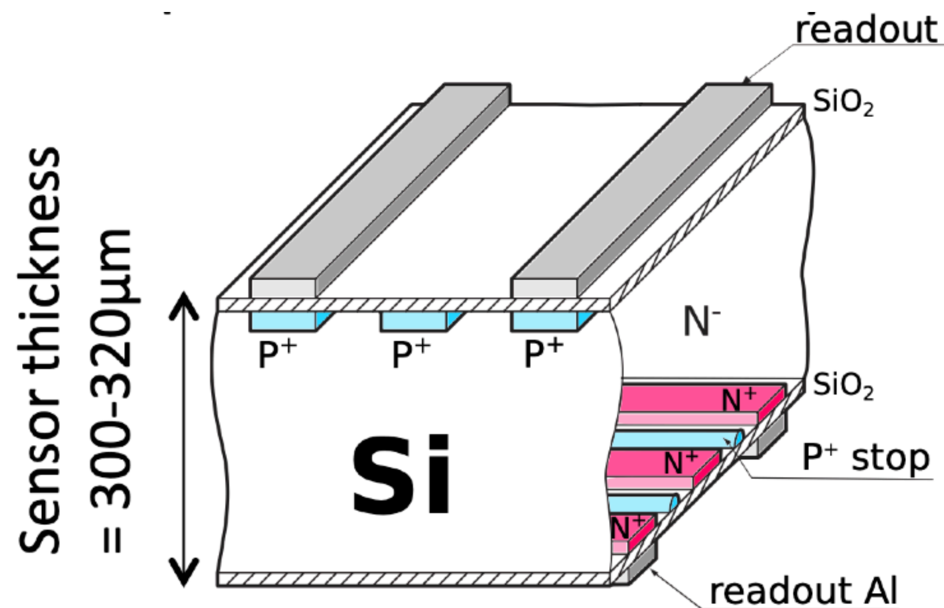
- Start at 2019
  - https://rd.kek.jp/platform/platform_index.html

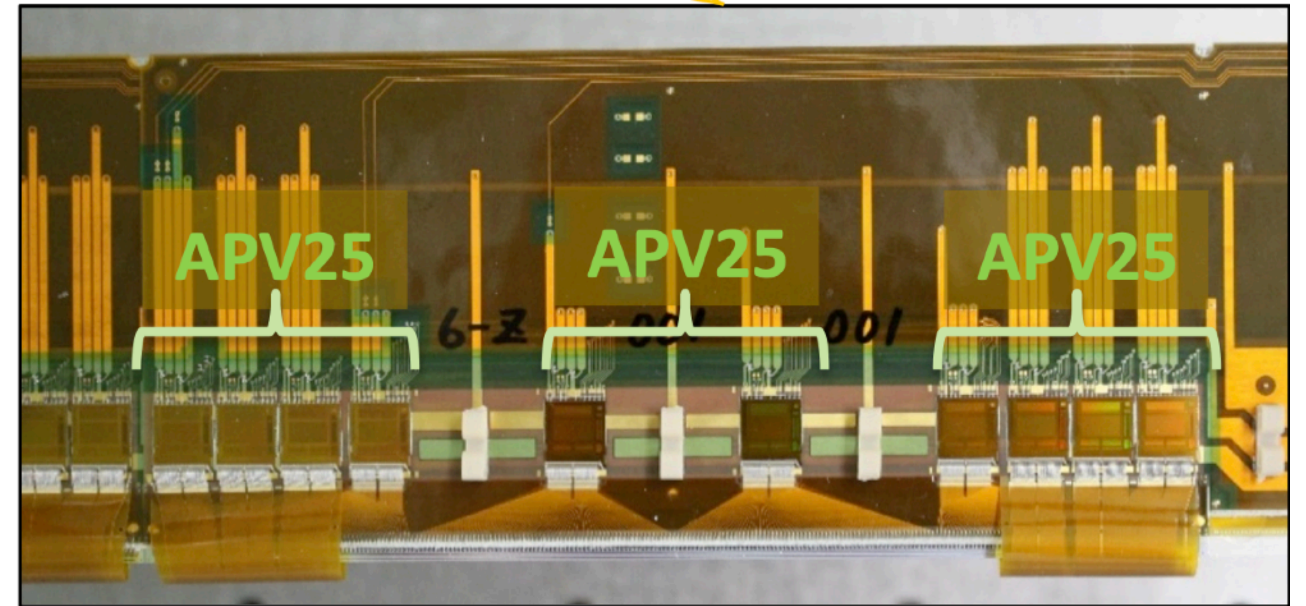
- Group B : silicon detector
  - https://research.kek.jp/people/togawa/RD-platform-Si/

Silicon strip detector

Belle SVD

Slide @ KEK RD silicon

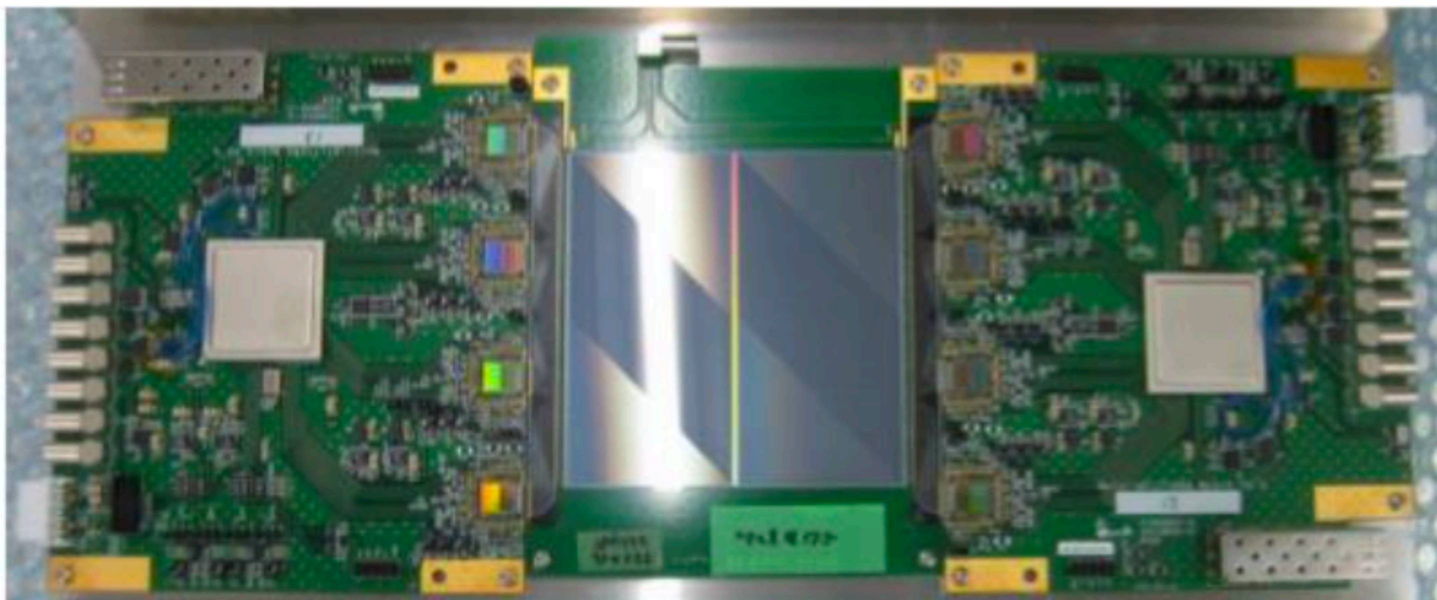




APV : Originally developed for the CMS experiment

g-2 SSD

Slide @ KEK RD silicon



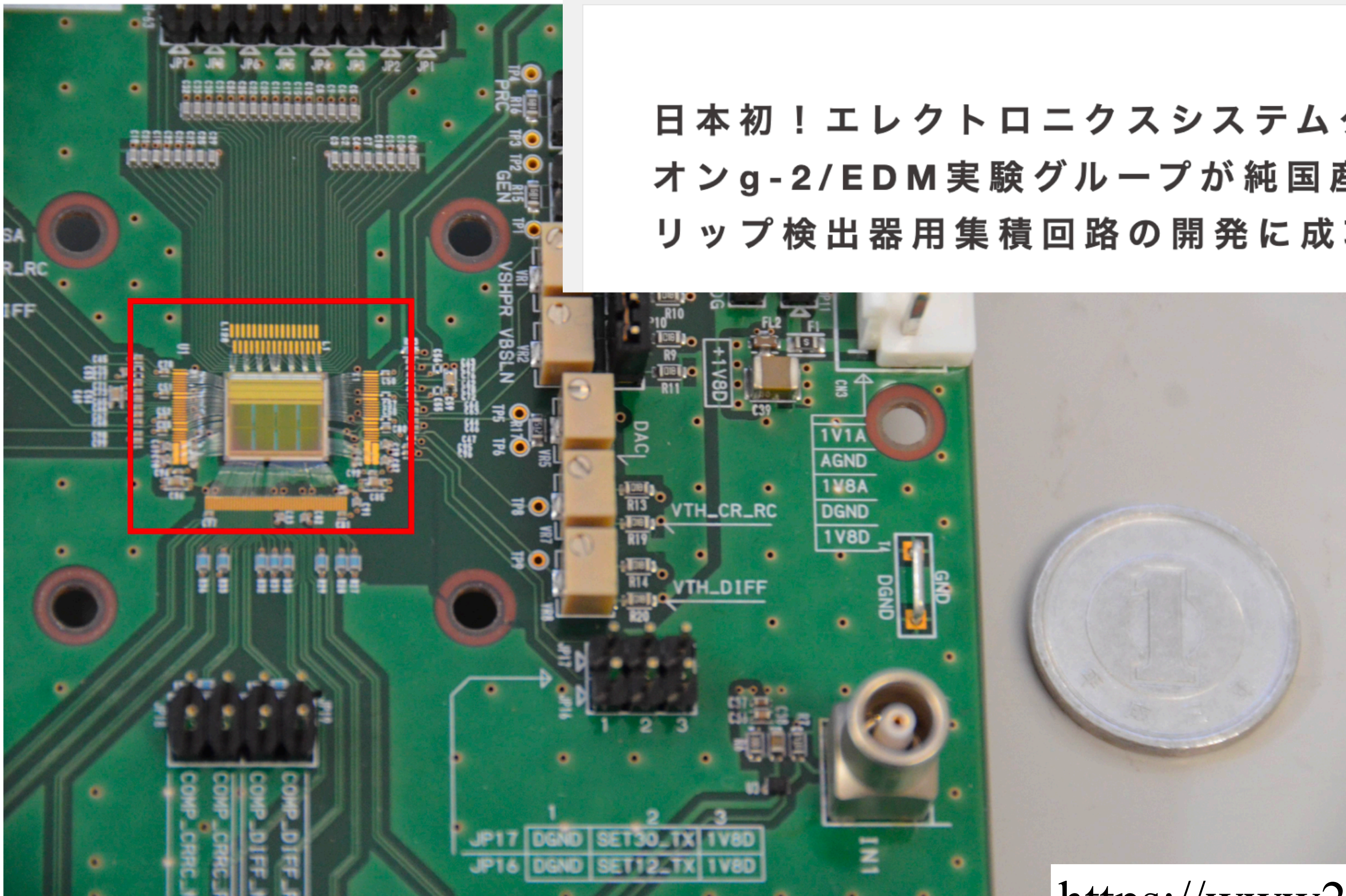
- First ASIC development in Japan!
- SliT128

ASIC Development

素粒子原子核研究所

宇宙をひもとく研究所

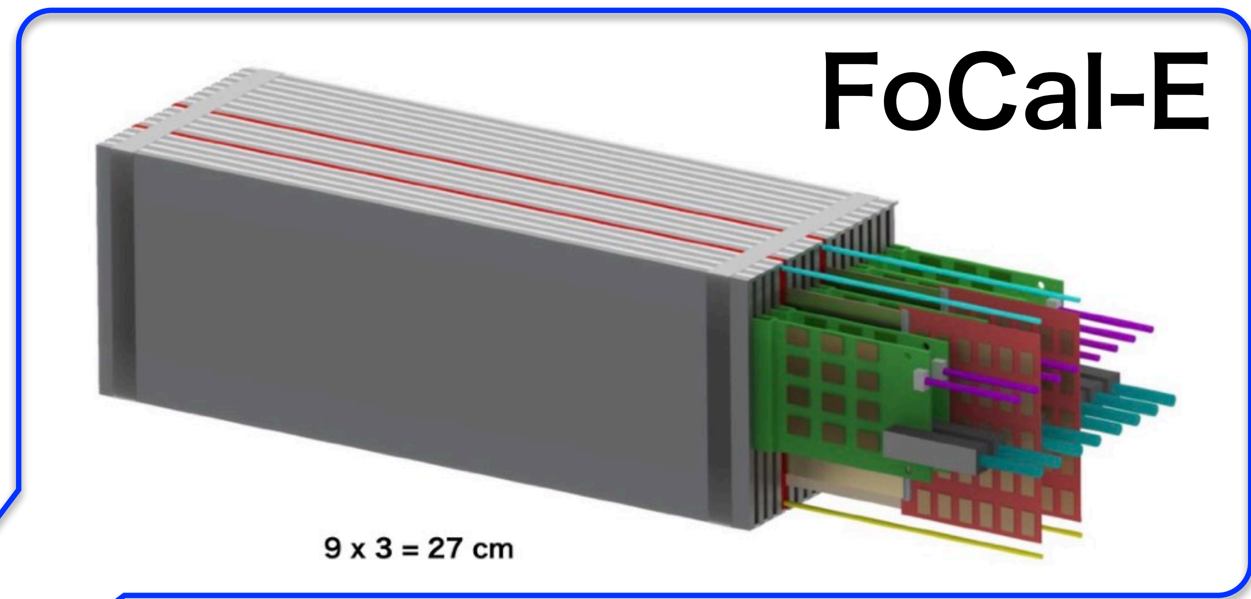
日本初！エレクトロニクスシステムグループとミューオンg-2/EDM実験グループが純国産シリコンストリップ検出器用集積回路の開発に成功

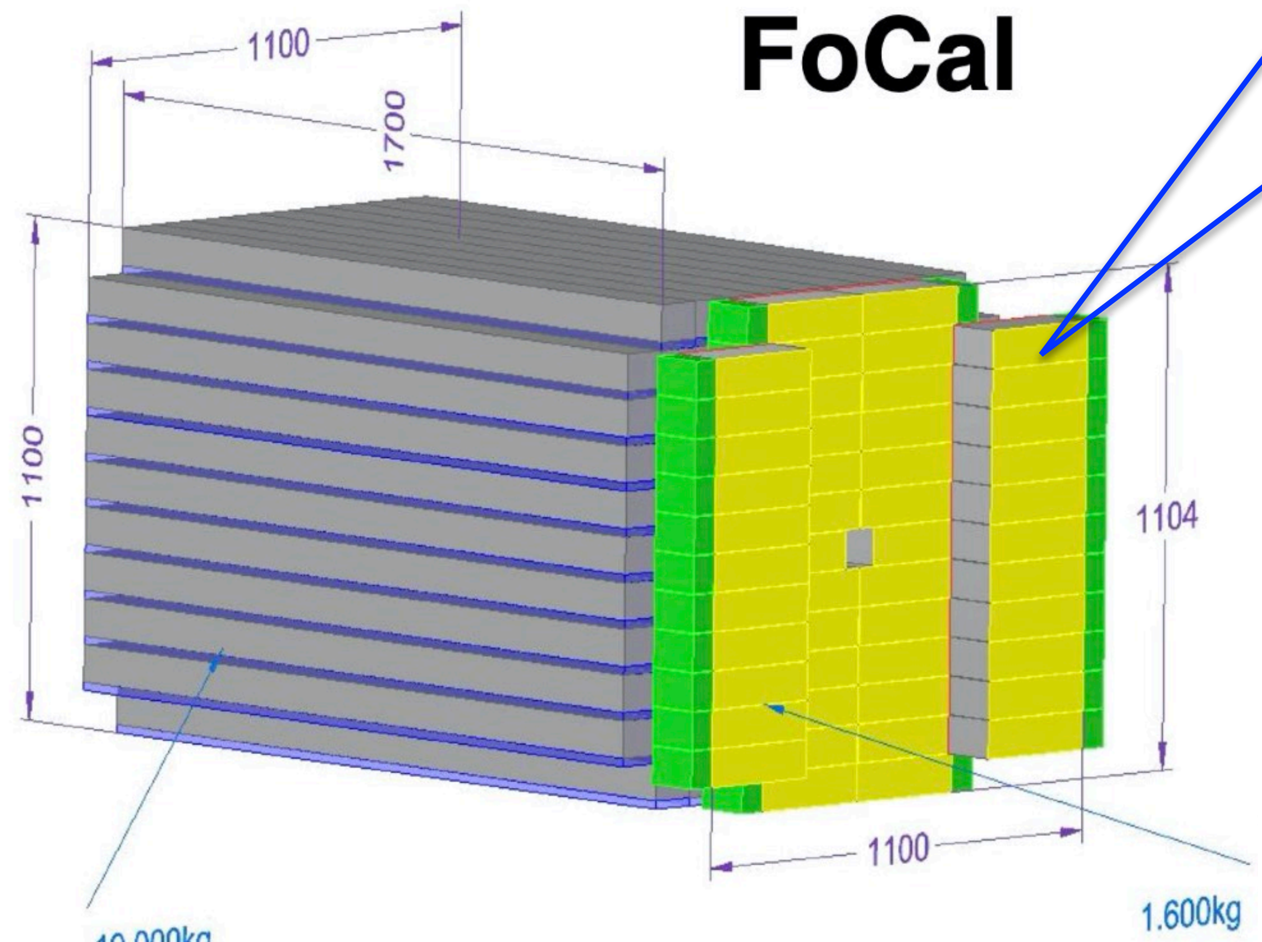


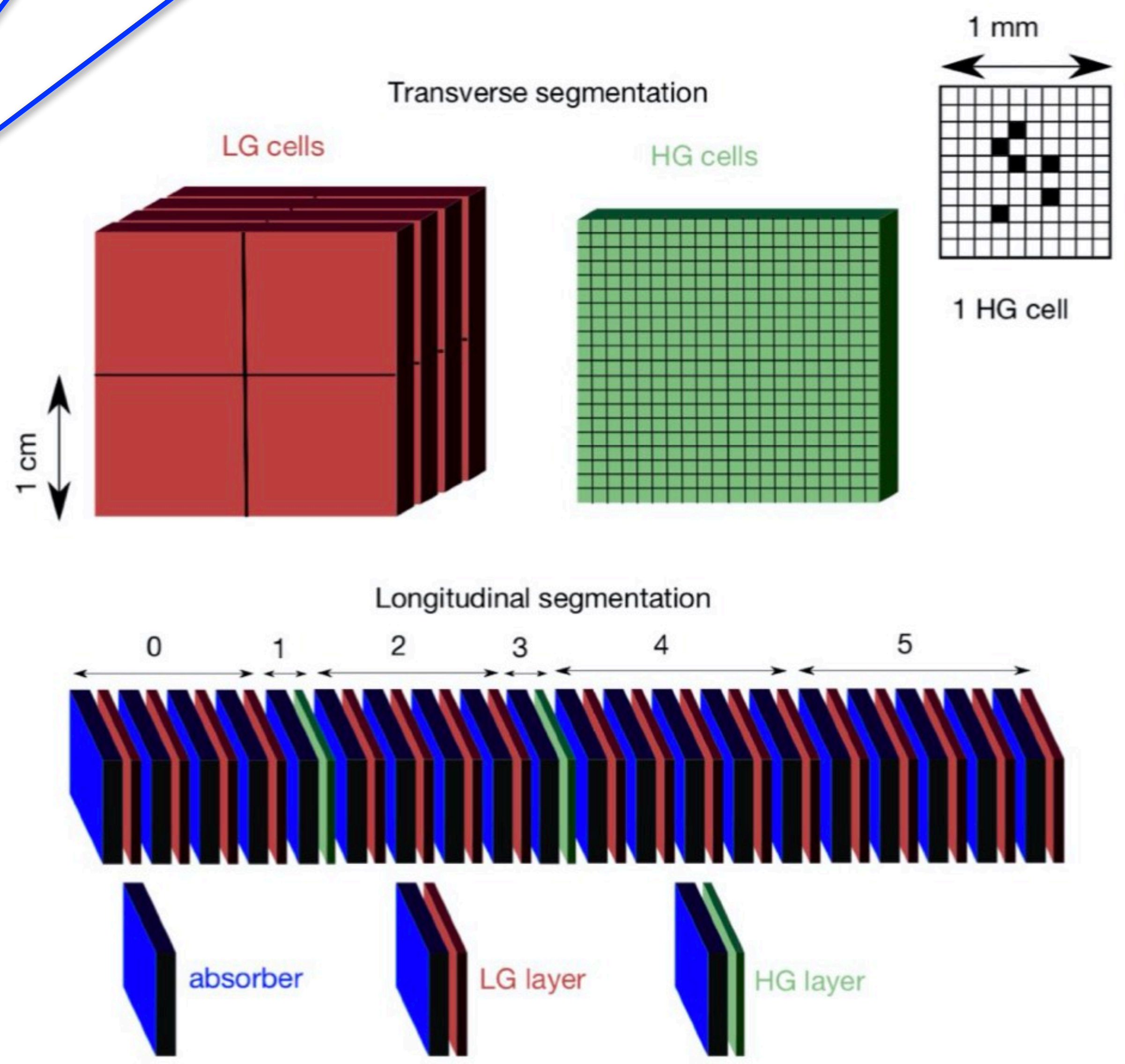
開発した集積回路（赤枠内）。1円玉の直径の半分ほど（1辺約1cm）と非常に小さいです。

https://www2.kek.jp/ipns/ja/post/2020/03/20200309/

ALICE FoCal Si-W Electro-Magnetic Calorimeter







- Discussion about "production" : https://kds.kek.jp/event/33450/

New material

- New characteristic beyond silicon !

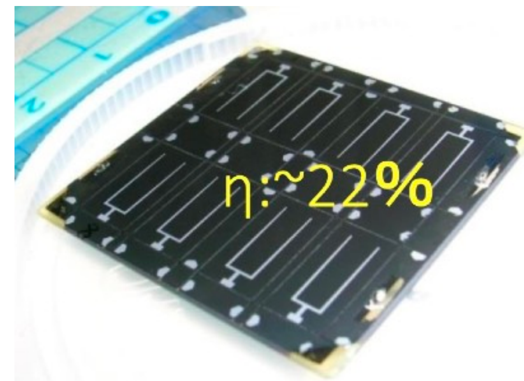
Wide-gap semiconductor

- Diamond, SiC, GaN..
- Tight binding is essentially radiation hard (bulk damage)
- Leakage current is significantly low
  - Can room temperature operation after radiation damage ?

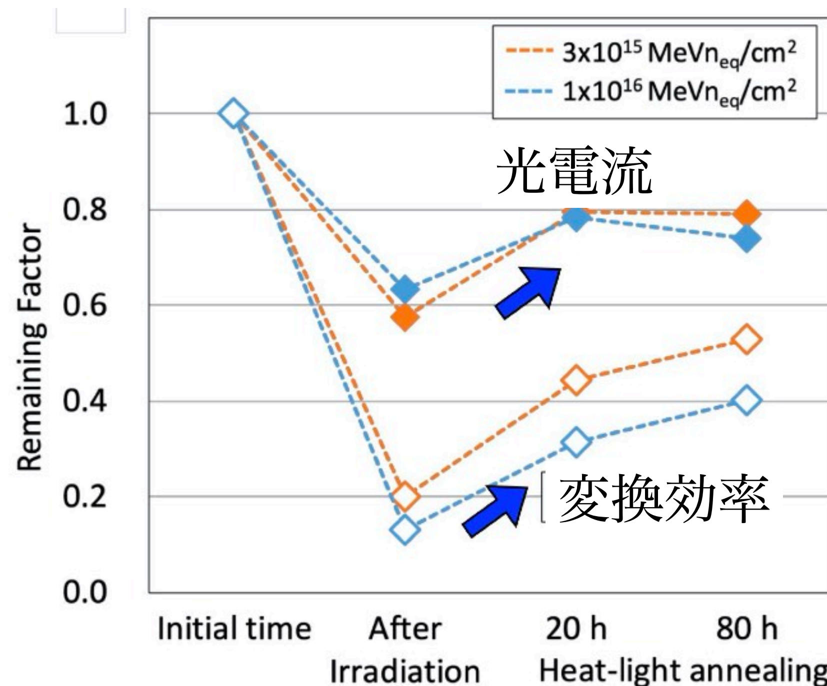
More detailed talk will be on RD platform workshop at 9/22 (Wed.) by Hajime Nishiguchi https://kds.kek.jp/event/38615/

Recovery type CIGS ($Cu(In,Ga)Se_2$)

Annealing by sun light (1 Sun, 95°C)



70 MeV proton @CYRIC



Single alpha detection (first observation)

Slide @ KEK RD silicon

Conclusion

- Silicon tracker play an impotent role for recent collider experiment
- Many technologies has been developed for experimental requirements
  - Hybrid type : Planer, 3D
  - Monolithic type : CMOS, SOI
  - Very precise timing detector : LGAD
- KEK RD platform, Group B, has started at 2019.
  - Many activities are on going.
  - Please join if you are interested in the semiconductor detector !
  - Next RD platform workshop at 9/22 (Wed.)
    - https://kds.kek.jp/event/38615/

Backup

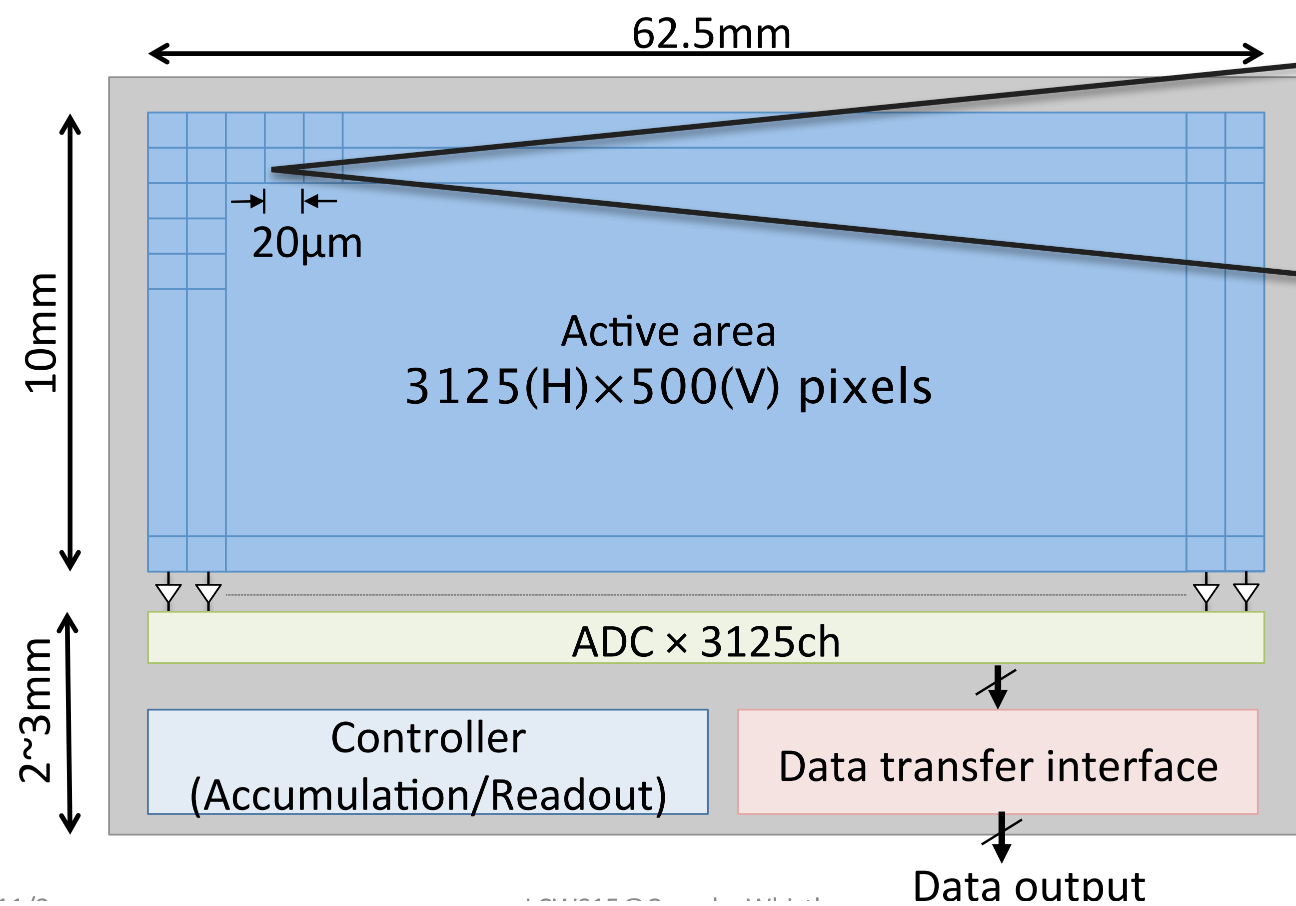
Radiation damage

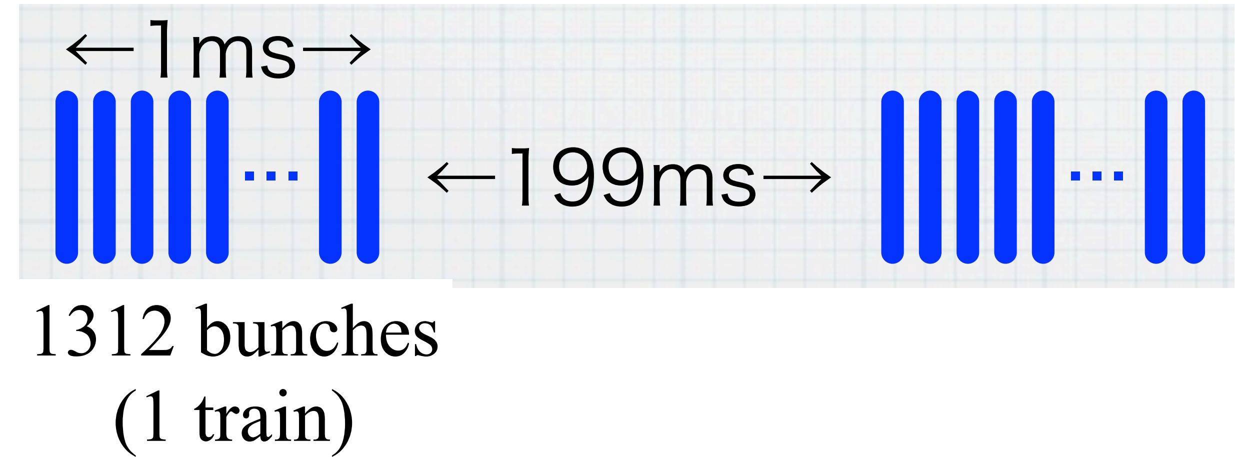
- TID (Total Ionization Doze) : Interaction with electron
  - Energy loss by ionization. Charge is built up at border.
    - Charged particles : electron (photon), proton ..
    - Unit : Rad, Gy

- NIEL (Non Ionization Energy Loss)：Interaction with nuclei
  - Kick-out effect of nuclei. Lattice defect is increased.
    - Heavy particles : neutron, proton ..
    - Unit : 1 MeV n_{eq} / cm^2

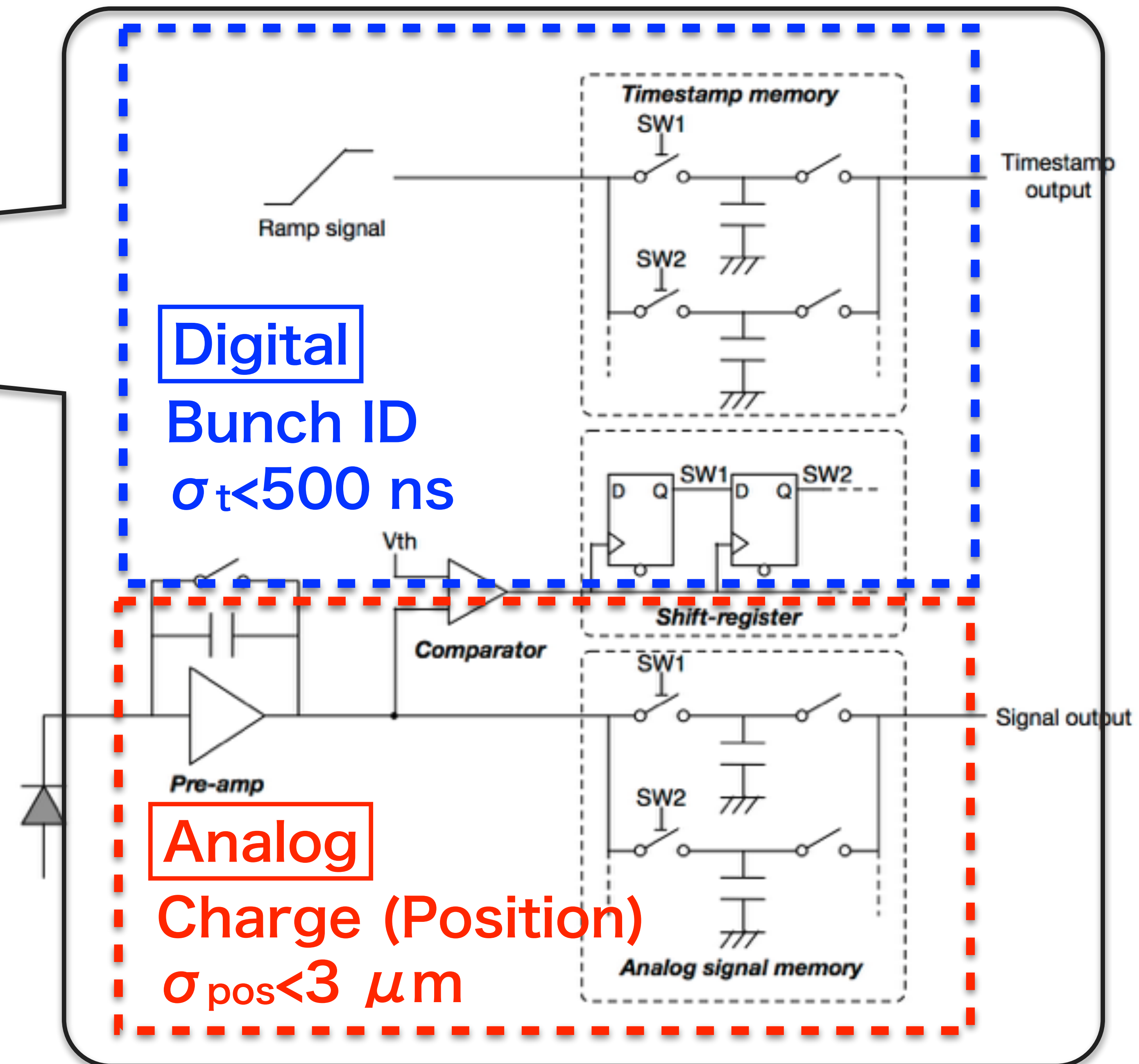
SOFIST
(SOI for Fine Measurements of Space and Time)

Proposing design



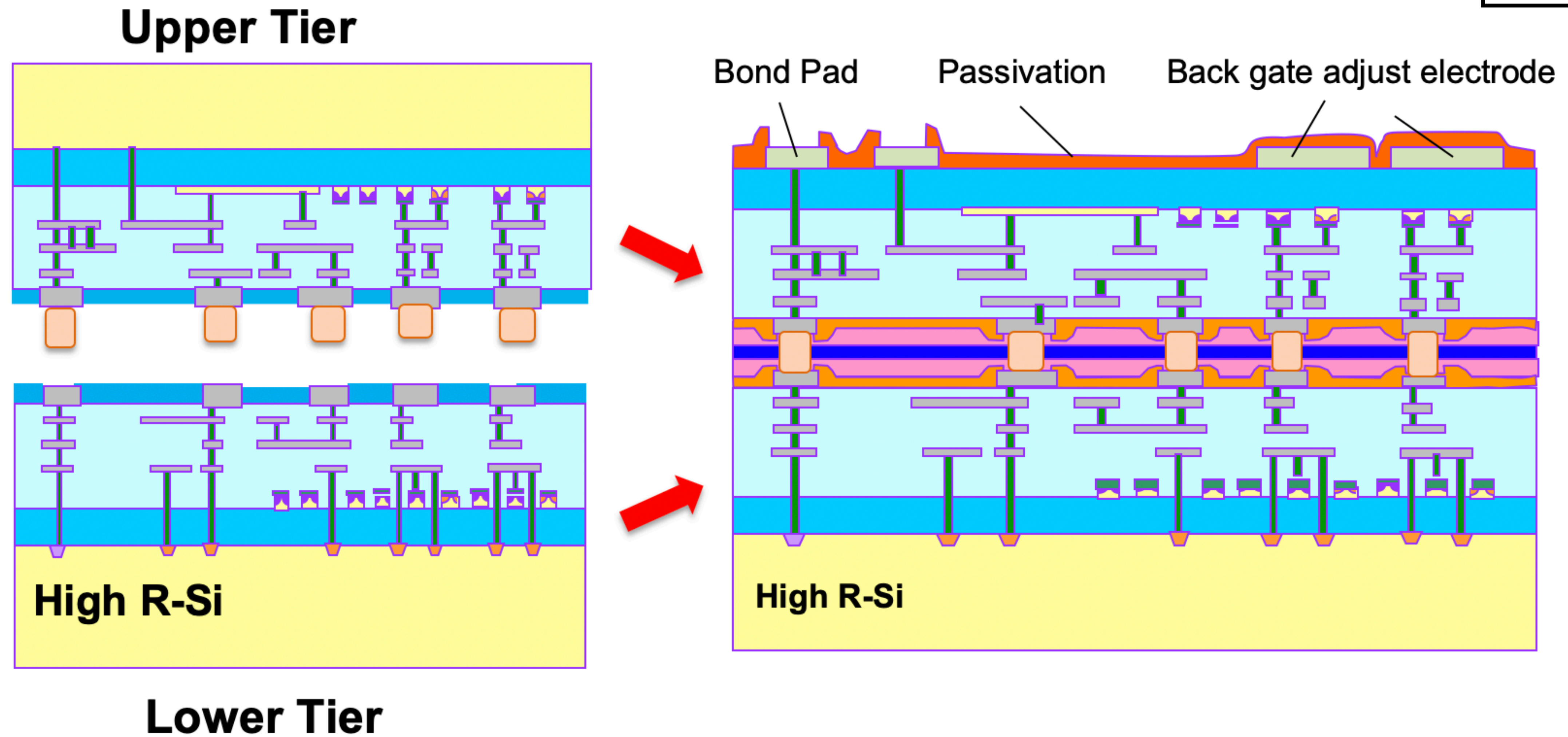


1312 bunches
(1 train)



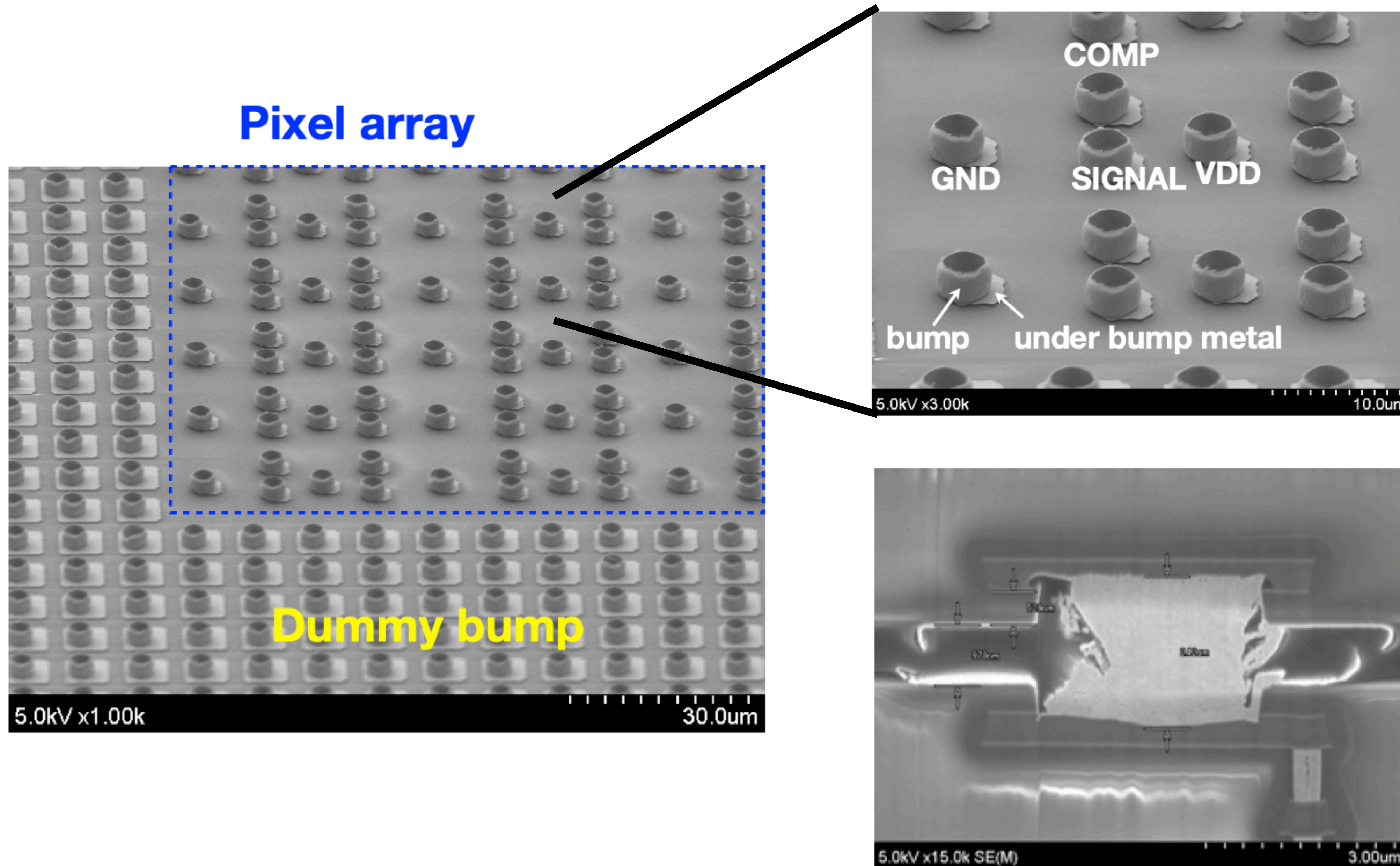
Pixel size = 20 x 20 μm^2
Thickness = 50 µm

SOI : More circuit..
3D vertical integration



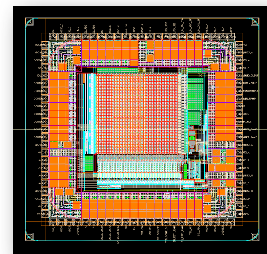
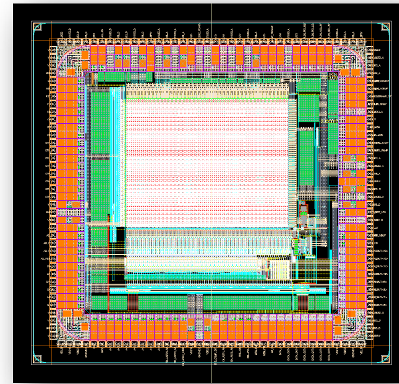
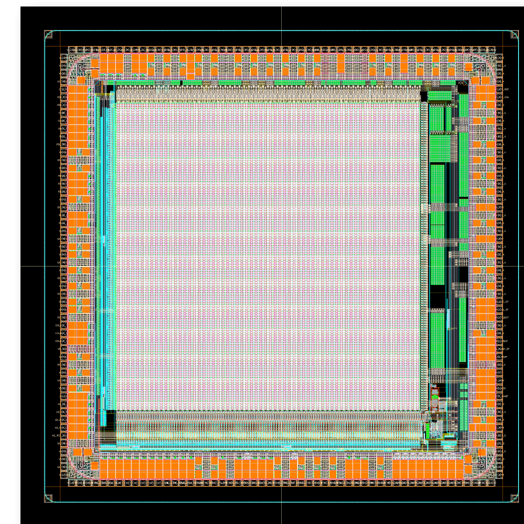
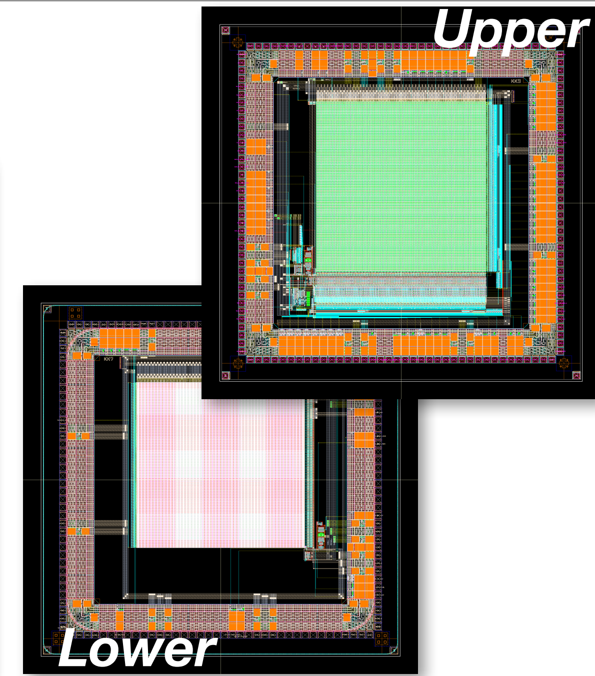
- For SOFIT v.4
- Upper and Lower Tier chips are produced in a same wafer and bonded chip to chip.

SOI : More circuit..
3D vertical integration

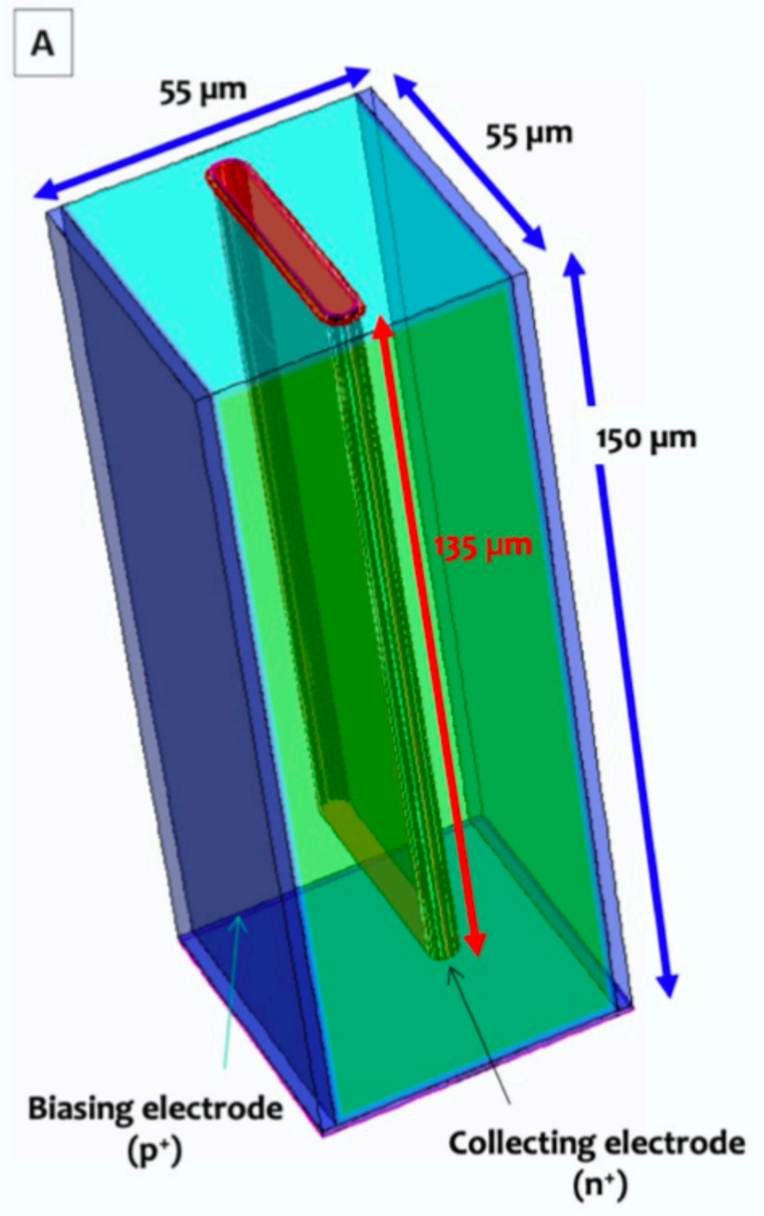


- For SOFIT v.4
- Upper and Lower Tier chips are produced in a same wafer and bonded chip to chip.

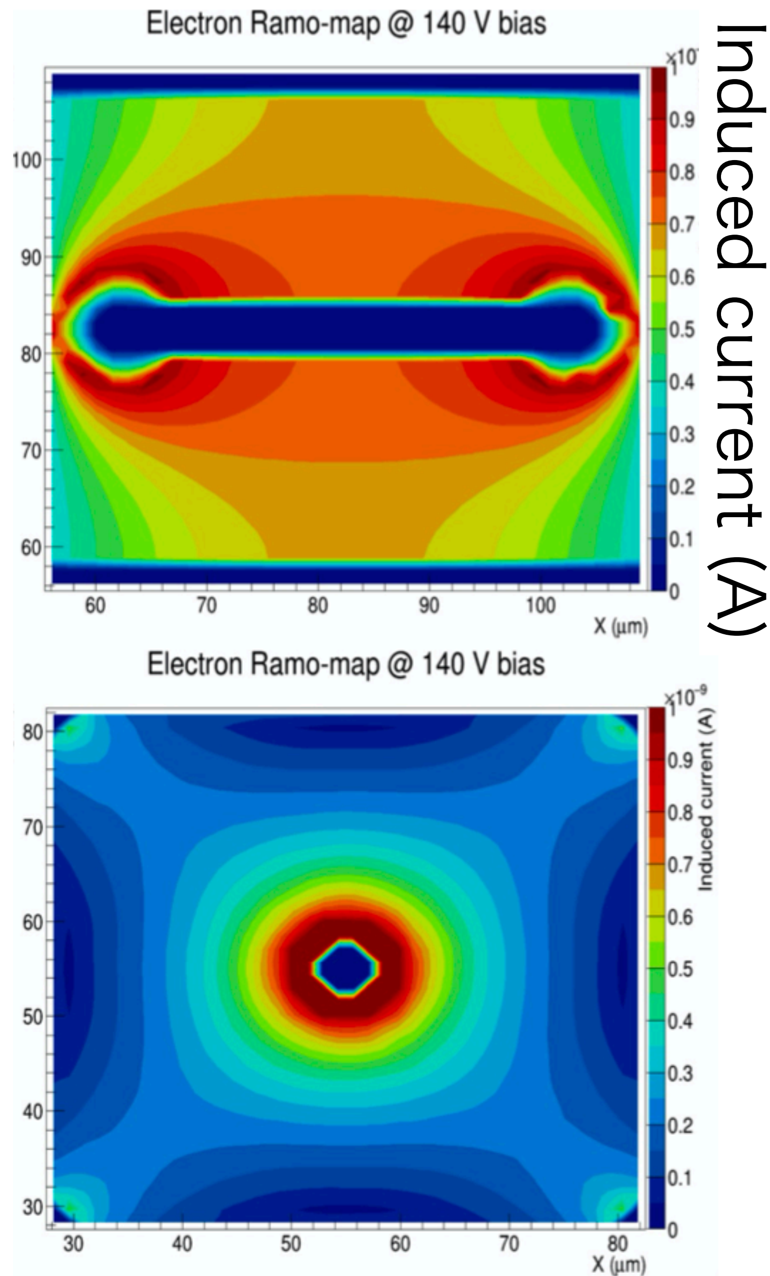
SOFIST

	MX1850	MX2040	MX2166	
SOFIST	ver.1	ver.2	ver.3	ver.4 (3D)
				
Chip Size (mm^2)	2.9 × 2.9	4.45 × 4.45	6 × 6	4.45 × 4.45
Pixel Size (μm^2)	20 × 20	25 × 25	30 × 30	20 × 20
Pixel Array	50 × 50	64 × 64 (Time Stamp) 16 × 64 (Analog Signal)	128 × 128	104 × 104
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n*-type (Single SOI)	Cz *p*-type (Double SOI)	FZ *p*-type (Double SOI)	FZ *p*-type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Under evaluation	Delivered (Jan. 2017)	Submitted (Jun. 2017)	Submitted (Jun. 2017)

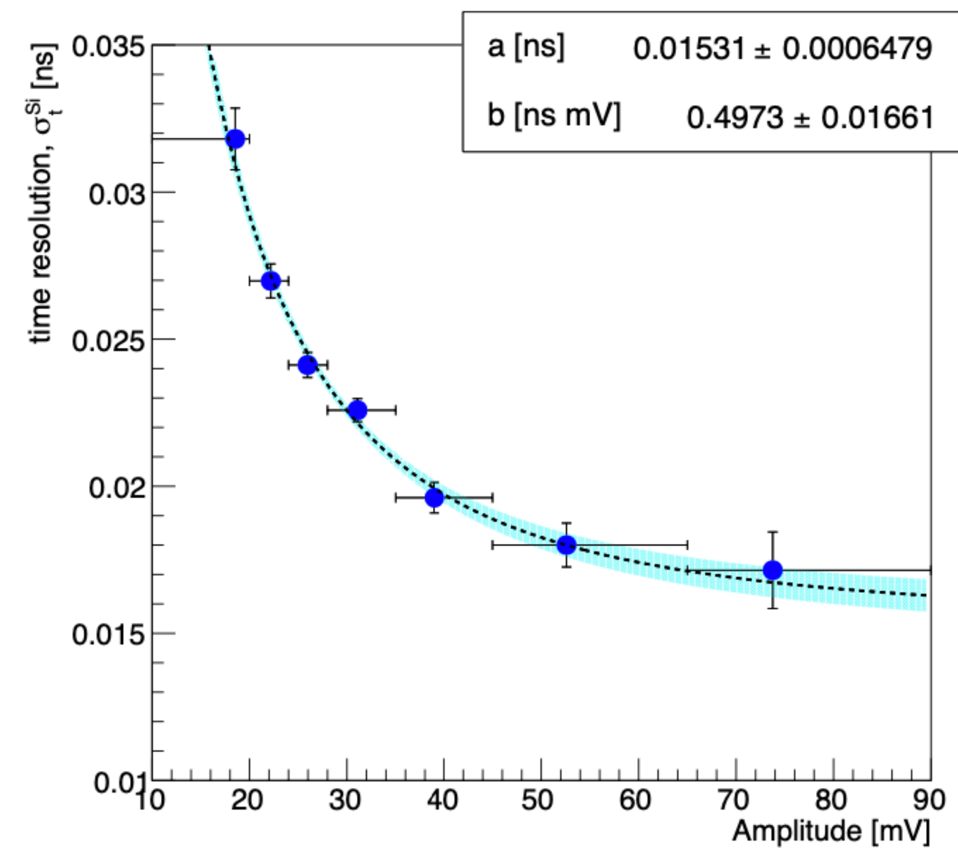
Timing resolution   TimeSPOT (3D)



Trench shape electrode



Ramo potential



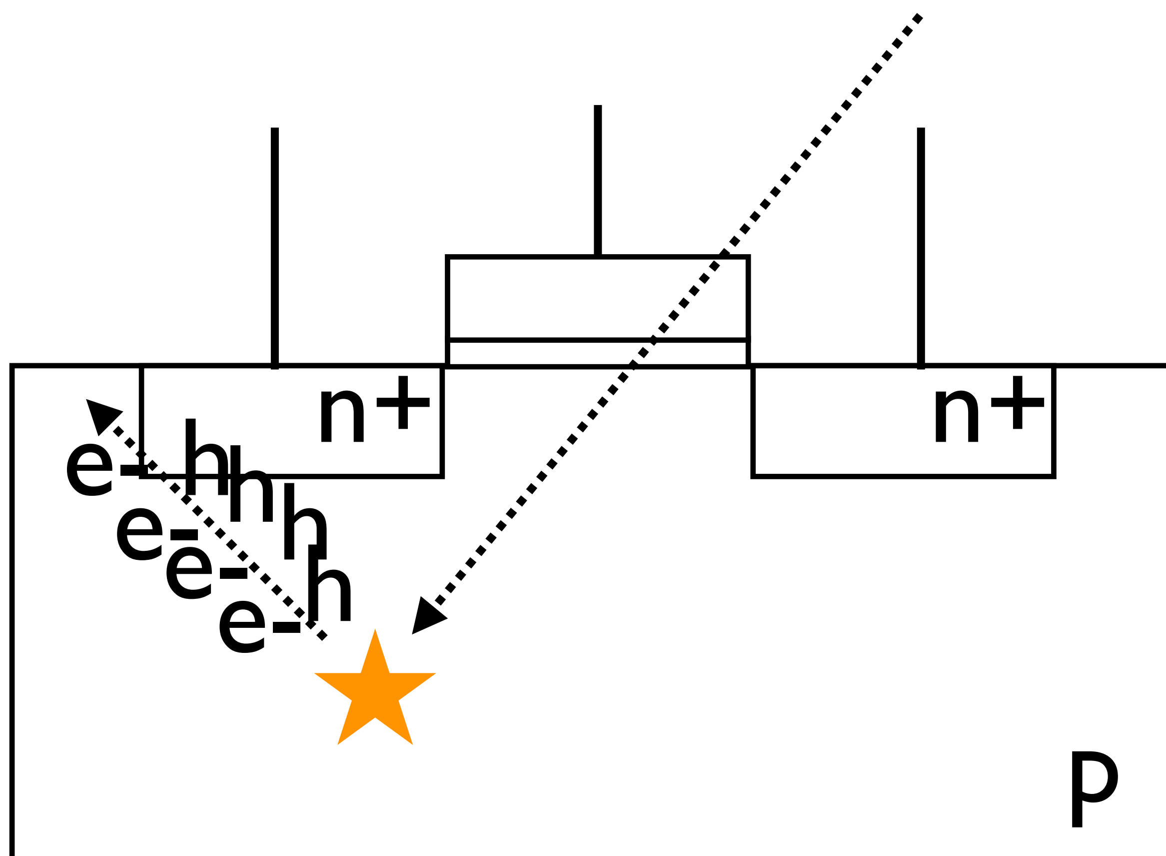
Achieved ~ 20 ps !
with test structure

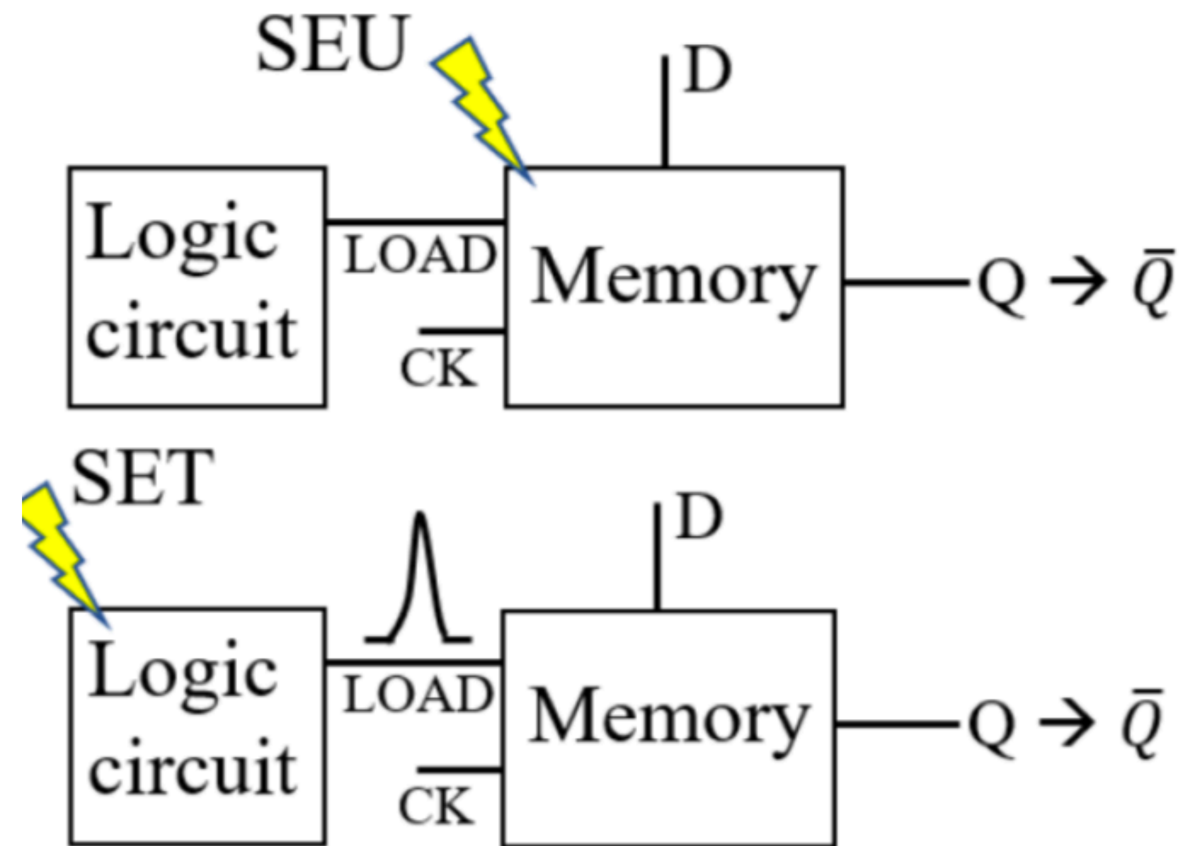
arXiv:2004.10881

Radiation damage on ASIC : Single Event Effect (SEE)

Large current by the secondary particles flips bit on memory.

Single Event Upset

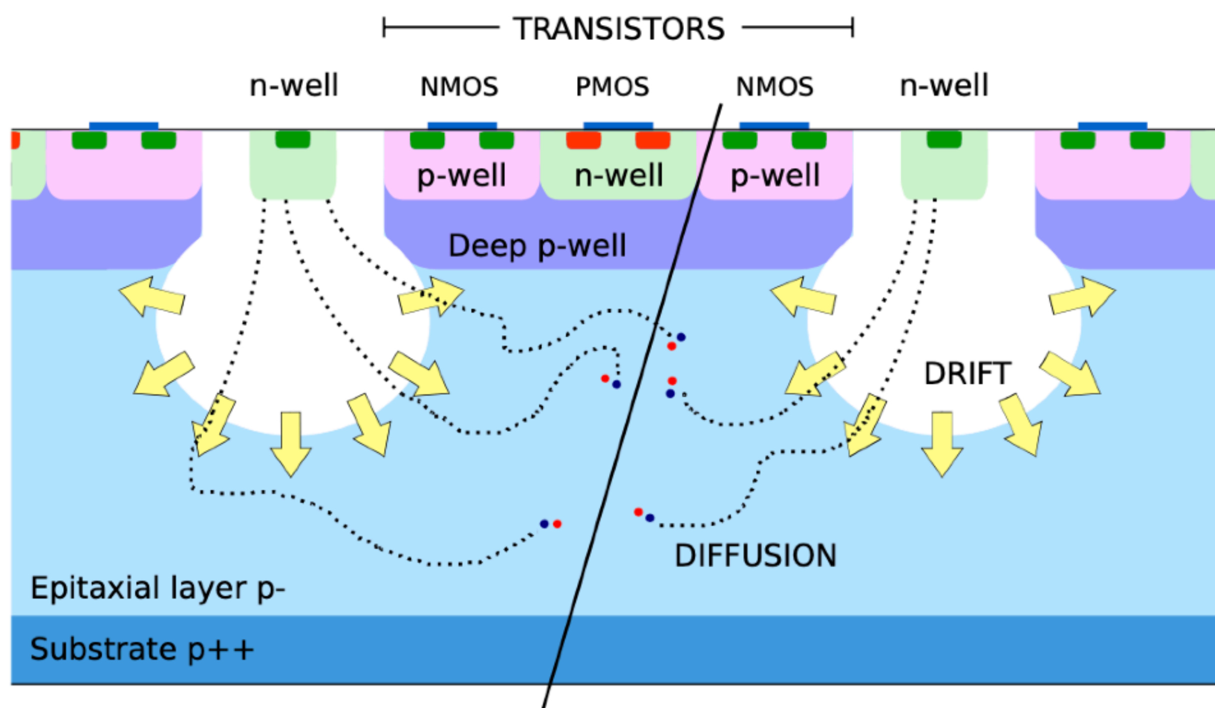


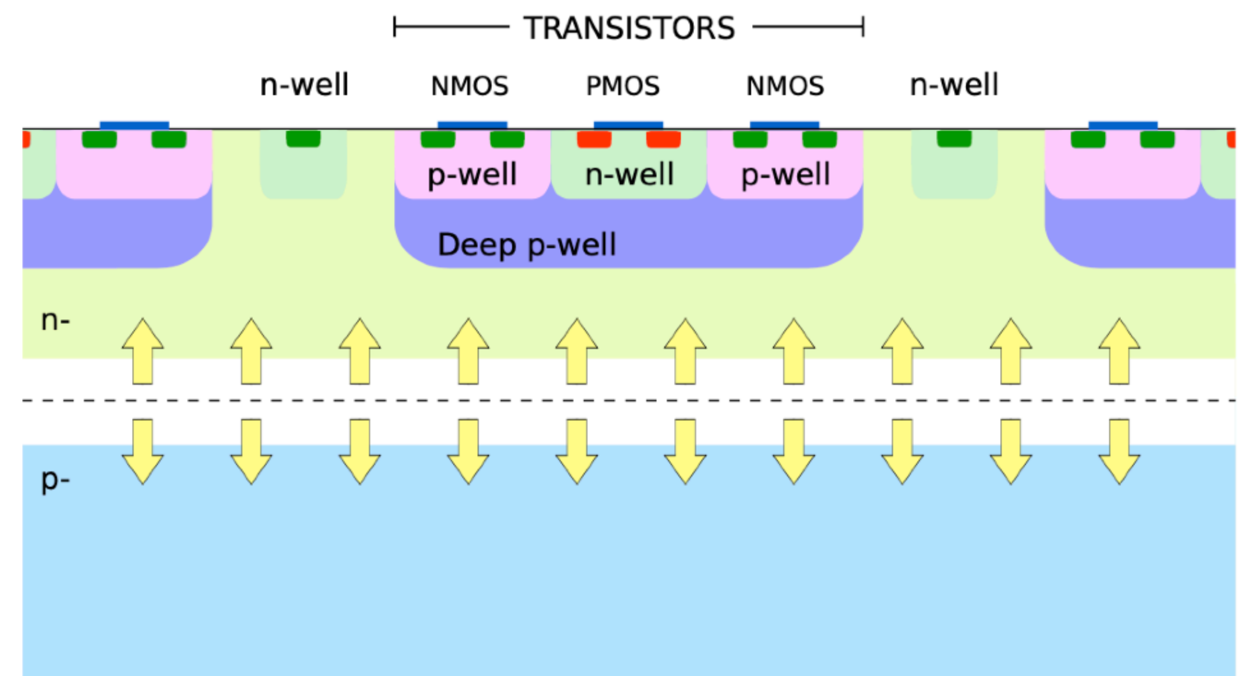


Single Event Transient

Unknown behavior of ASIC and FPGA by reprograming

CMOS : Modified small fill factor for ALICE ITS





- Add new n-layer between sensor and circuit layer.
  - Uniform depletion

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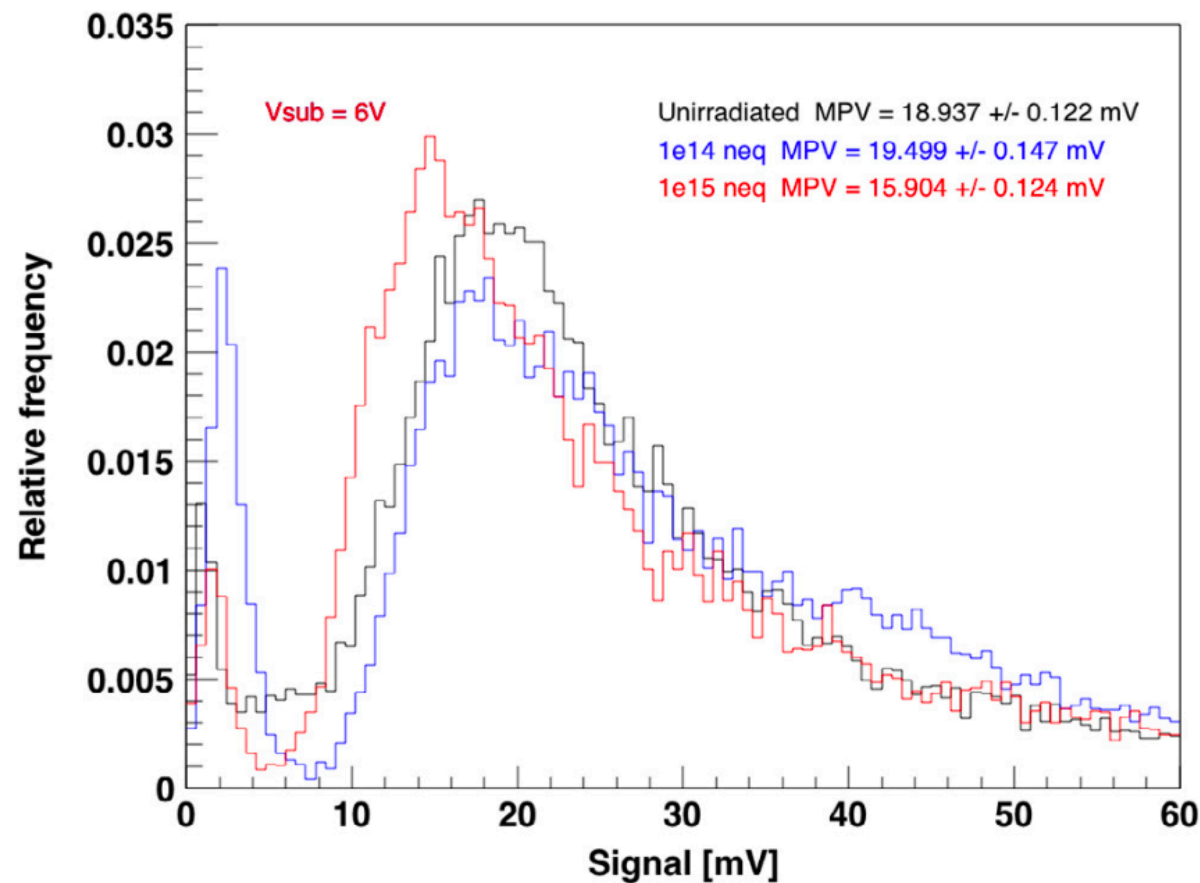
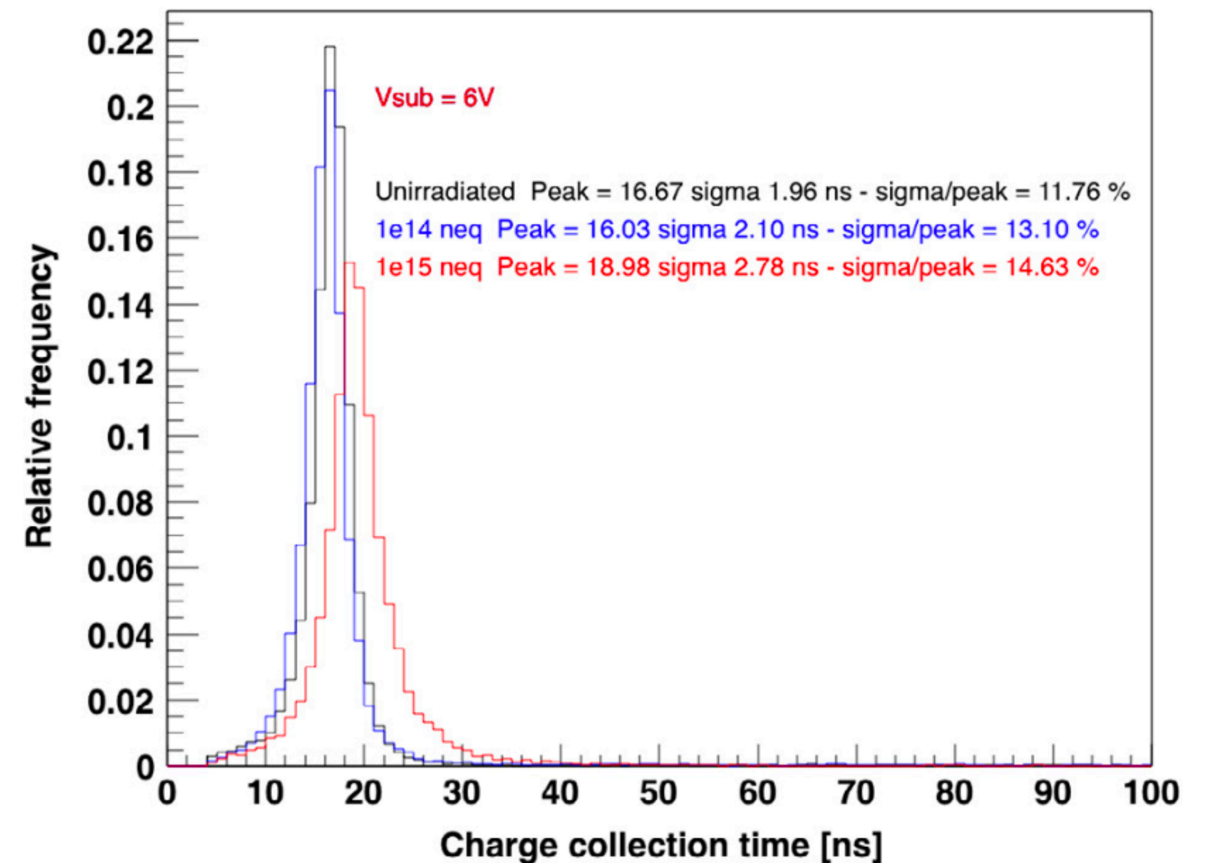
CMOS : Modified small fill factor for ALICE ITS





- Good charge collection and also timing !
  - Not so much changed after irradiation up to 1x10^{15} (1 MeV $n_{eq.}$/cm^2)
- Different modified structures in terms of rad. hard have been tried.
  - See Heinz Pernegger' talk.

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