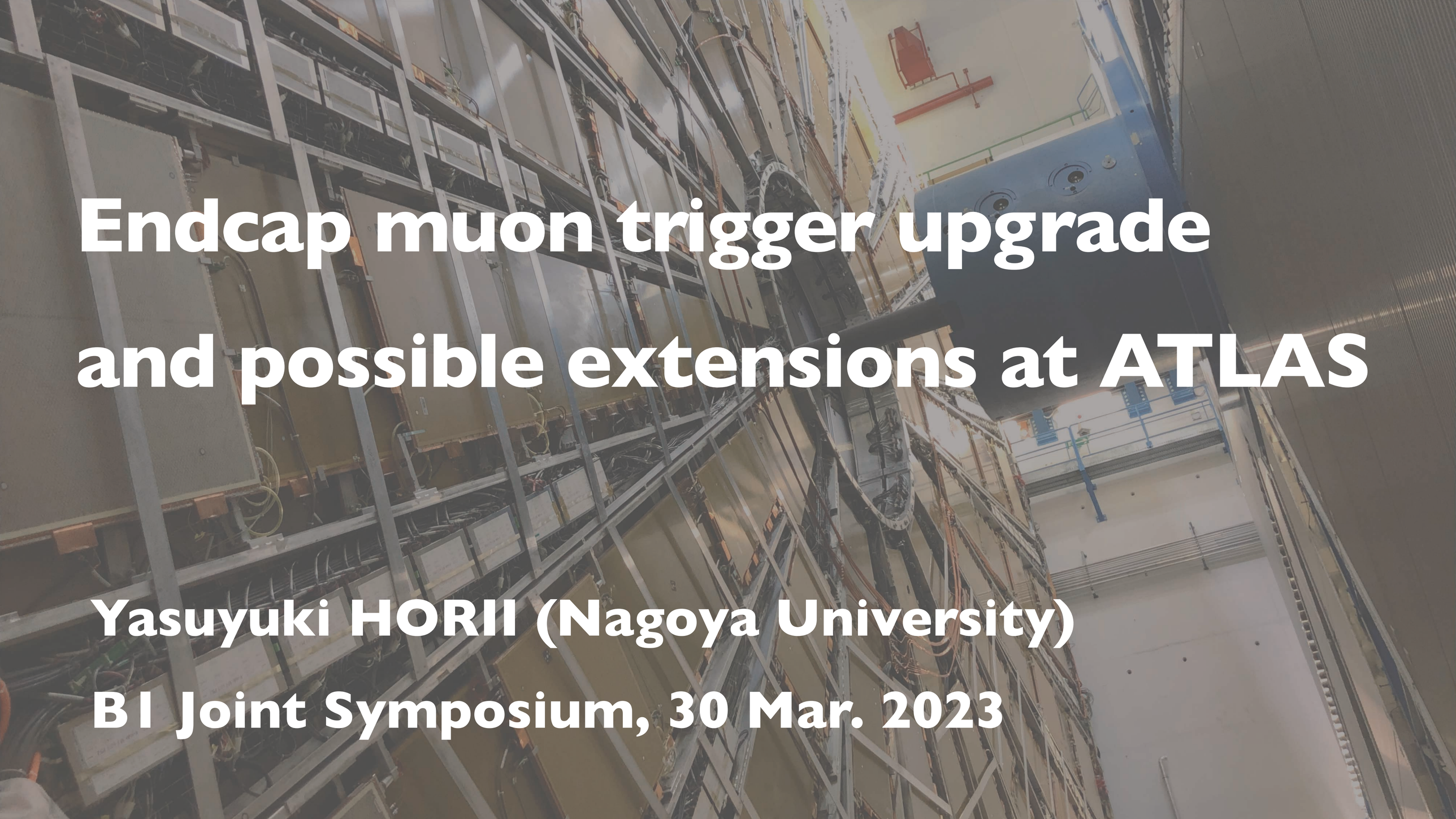
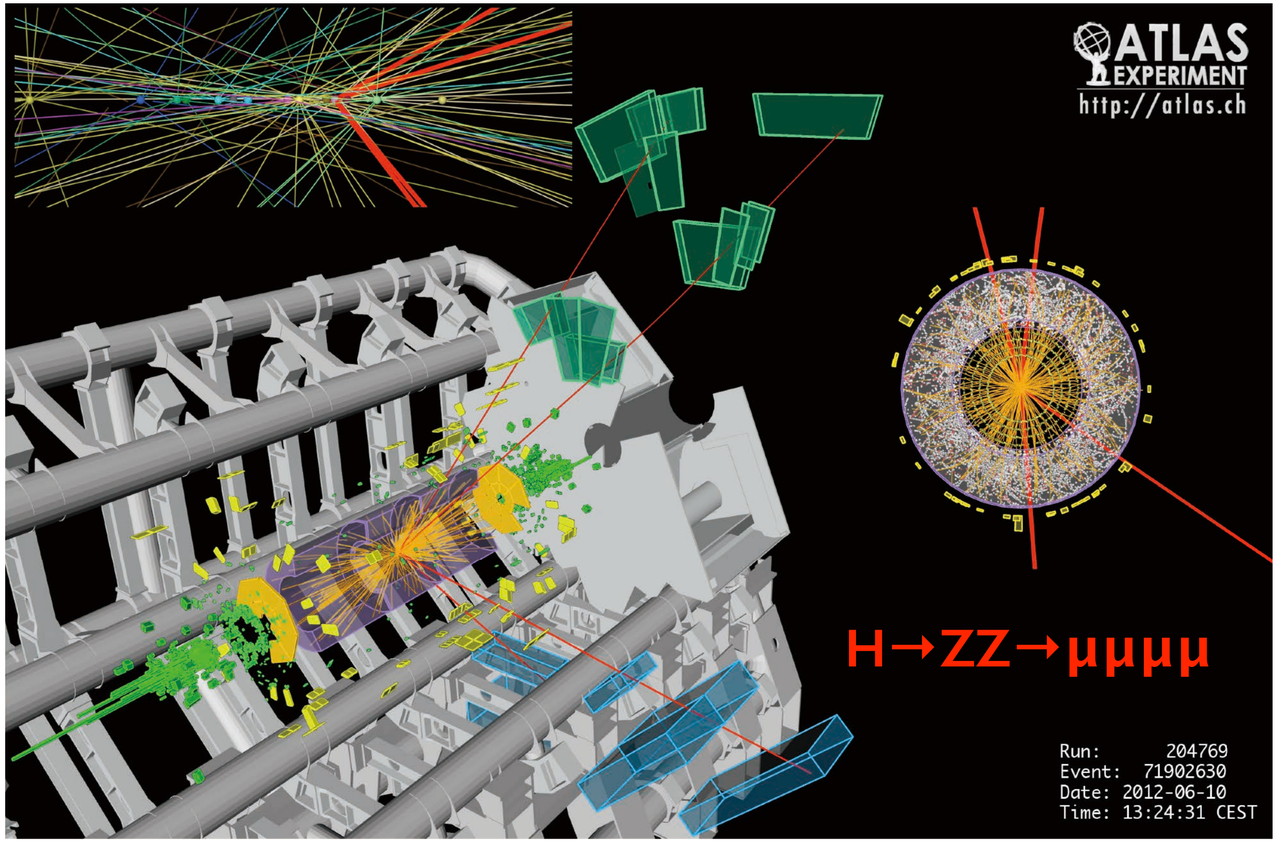


Endcap muon trigger upgrade and possible extensions at ATLAS

Yasuyuki HORII (Nagoya University)

B1 Joint Symposium, 30 Mar. 2023

Higgs Boson Observation in 2012



Chunichi, Oct. 2013

神の粒子 実験誇り

ノーベル物理学賞

参加の名大 歓喜

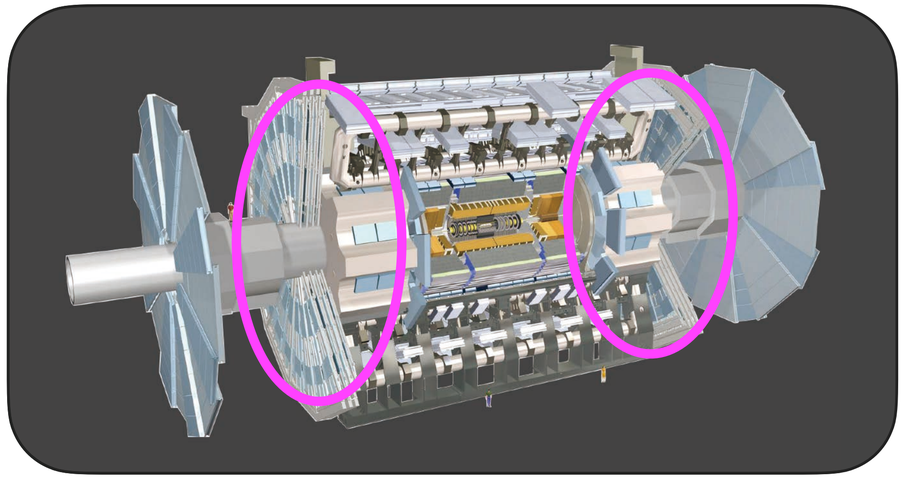
「必ずある 信じていた」

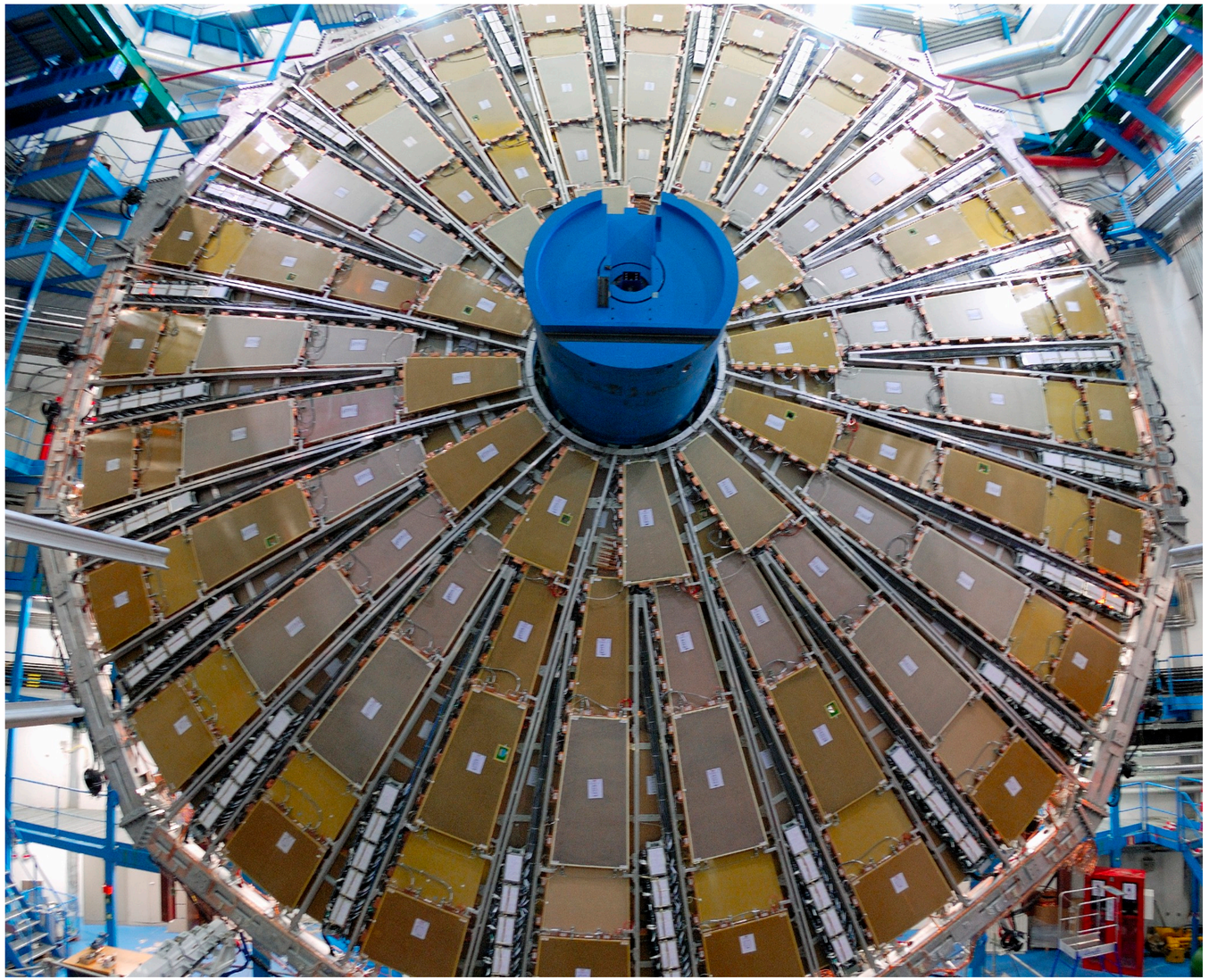
ノーベル物理学賞に「ヒッグス粒子」が決まり、笑顔を見せる戸本誠准教授（前列中央）と学生ら＝8日夜、名古屋市千種区の名古屋大で

日本も参加するアトラスチームの検出器＝CERN提供

Nagoya's Commitment: Thin Gap Chamber (TGC)

- Multiwire proportional chamber
- Primary role in muon trigger
- Height: ~25 m
- Channels: ~320,000





2022 — 10 Years after the Discovery

Article | Open Access | Published: 04 July 2022

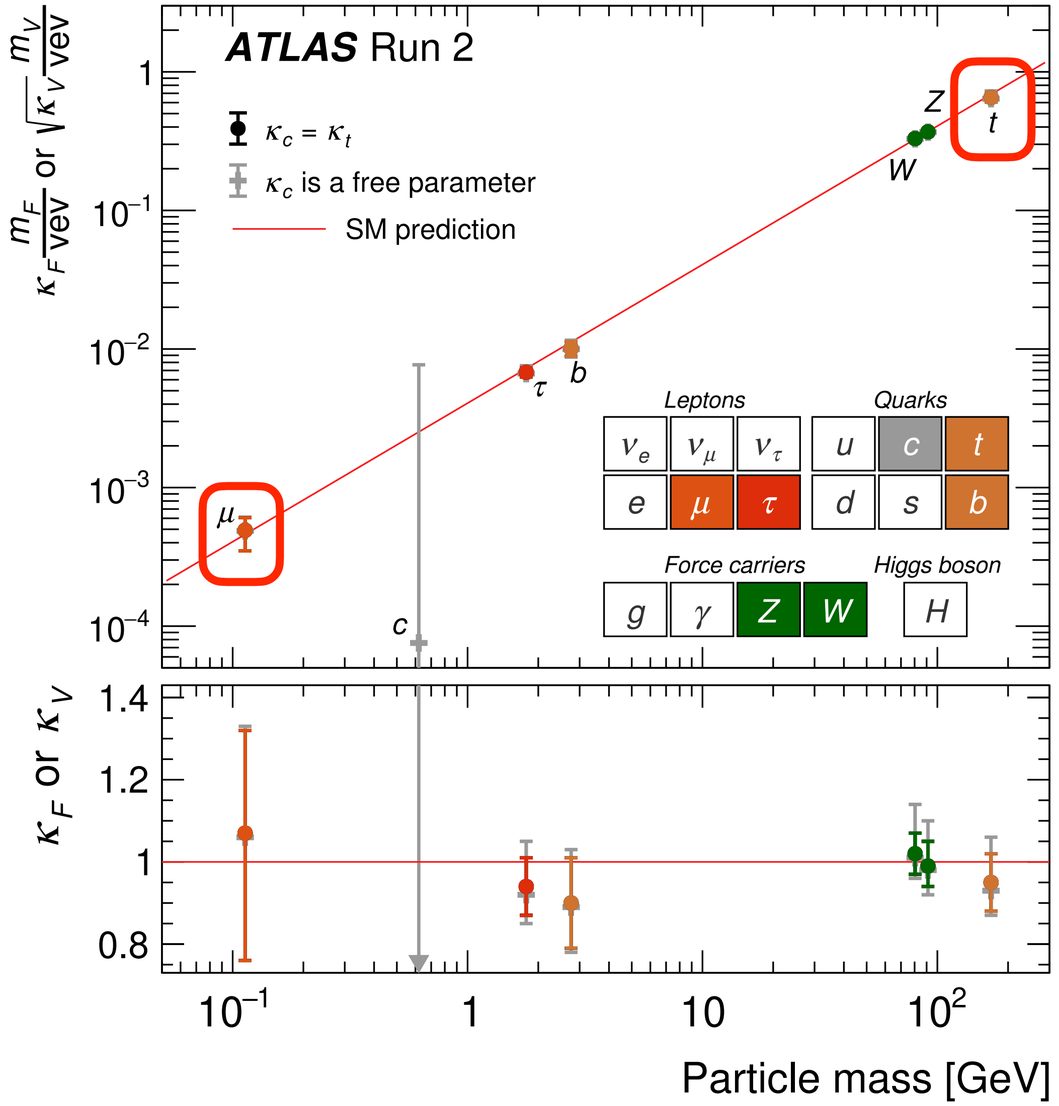
A detailed map of Higgs boson interactions by the ATLAS experiment ten years after the discovery

The ATLAS Collaboration

Nature **607**, 52–59 (2022) | Cite this article

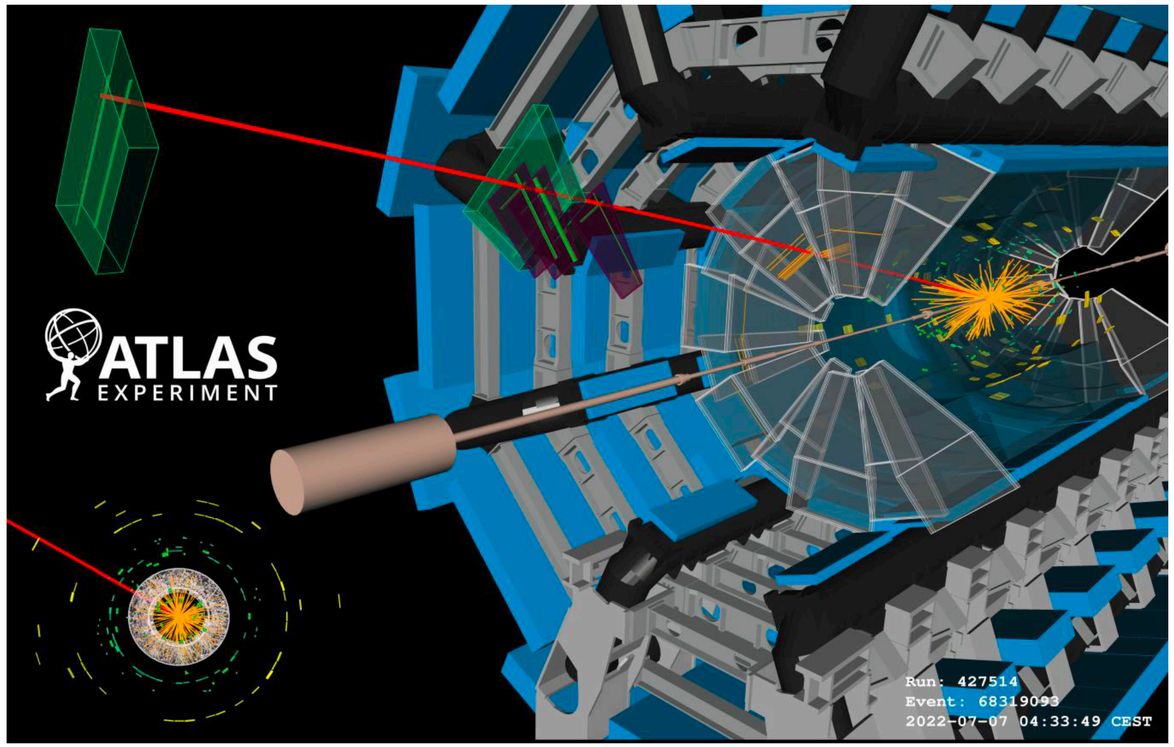
Symposium: https://home.cern/events/anniversary-discovery-higgs-boson

- **Higgs boson coupling observed (>5σ) for Z, W, t, b, and τ.**
- **Indication (2σ) for μ — more data needed**



Run 3 Started on 5 July 2022

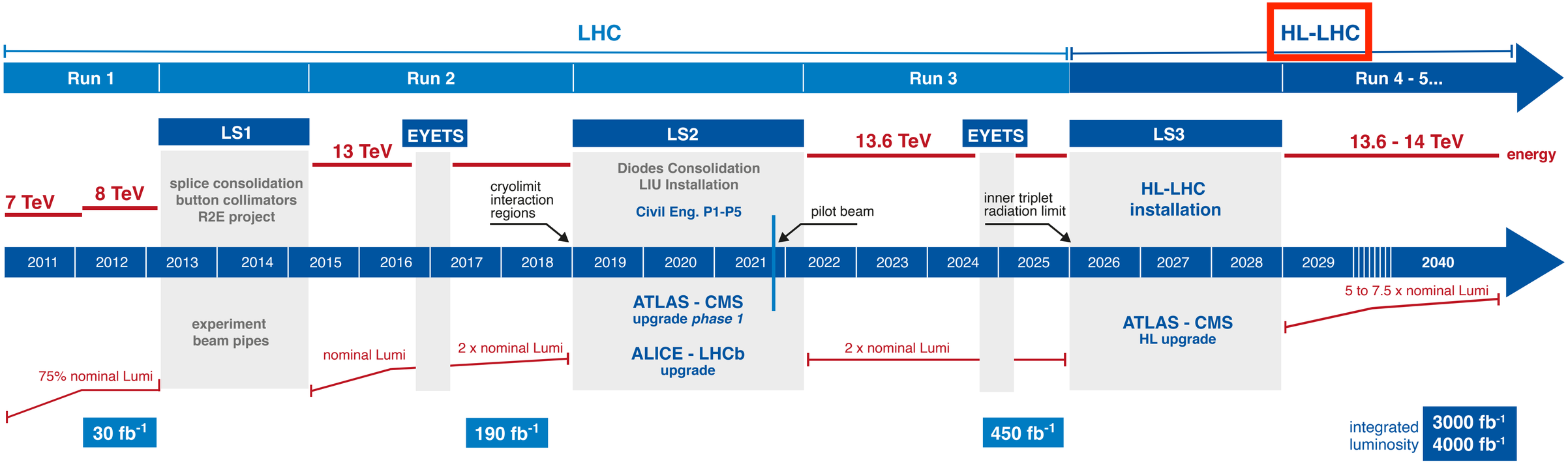
https://atlas.cern/Updates/Press-Statement/Run3-first-collisions



https://twiki.cern.ch/twiki/bin/view/AtlasPublic/EventDisplayRun3Collisions

Accumulation of data samples of proton-proton collisions at 13.6 TeV

Next — HL-LHC



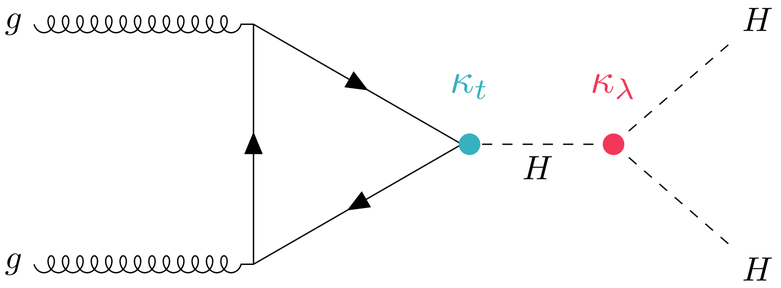
Luminosity upgrade: 2 x 10^{34} $cm^{-2}s^{-1}$ → 5–7.5 x 10^{34} $cm^{-2}s^{-1}$

Start of the operation in 2029

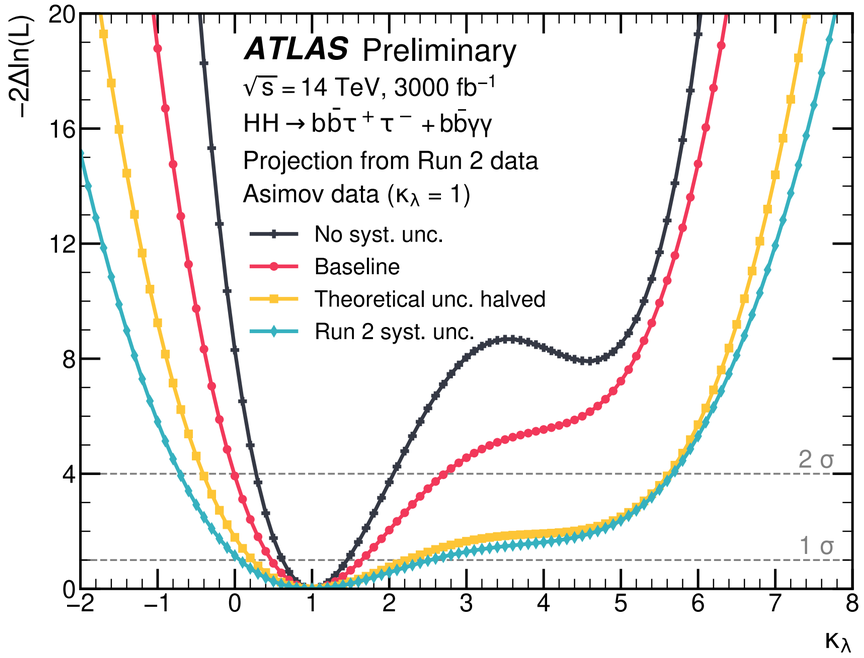
Physics Prospect for HL-LHC (Selected)

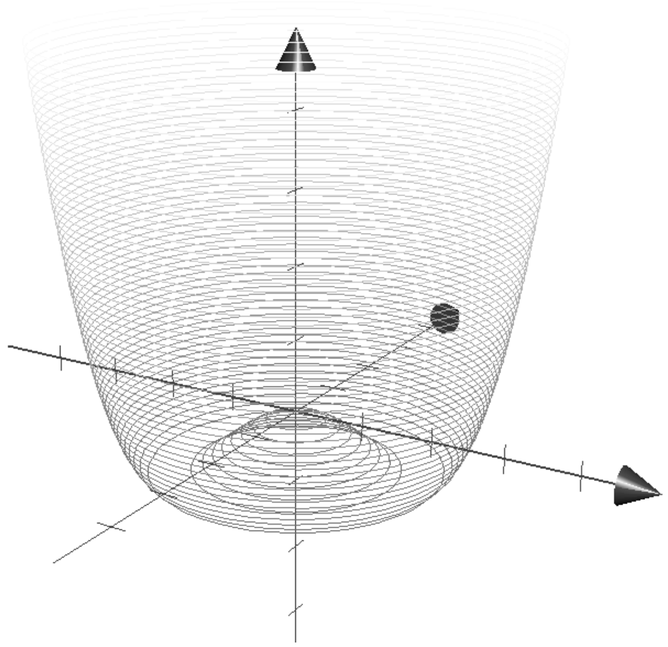
Di-Higgs production for self-coupling measurement

- **SM significance for ATLAS bbγγ + bbττ: 3.2σ (link)**
- **SM significance for ATLAS + CMS: 5σ (link)**



ATL-PHYS-PUB-2022-005





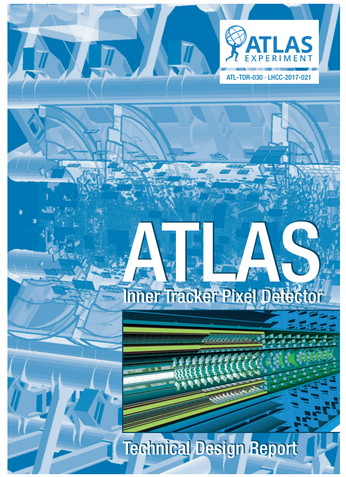
$$V(h) = \frac{1}{2}m_H^2 h^2 + \lambda_3 v h^3 + \frac{1}{4}\lambda_4 h^4$$

$$\lambda_3^{\mathrm{SM}} = \lambda_4^{\mathrm{SM}} = \frac{m_H^2}{2v^2}$$

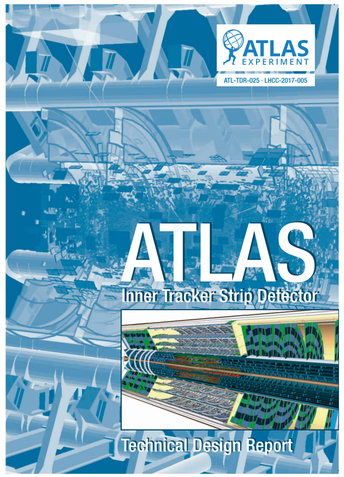
Direct constraint on Higgs potential!

Technical Design Reports (TDRs)

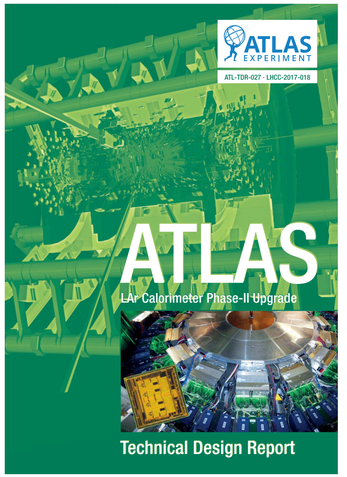
Six TDRs (~2600 pages) approved by CERN Research Board in Apr. 2018



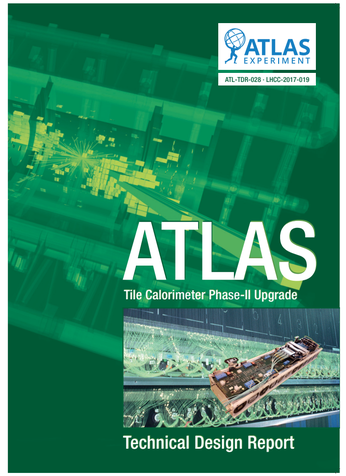
Inner Tracker
Pixel Detector
ATL-TDR-030
482 pages



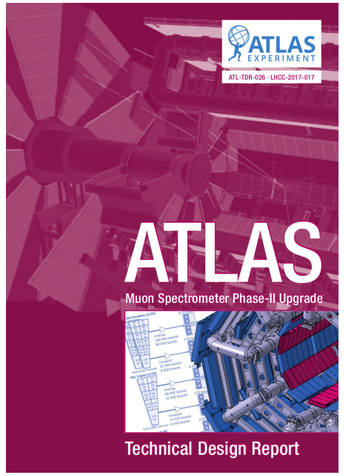
Inner Tracker
Strip Detector
ATL-TDR-025
556 pages



LAr Calorimeter
ATL-TDR-027
271 pages

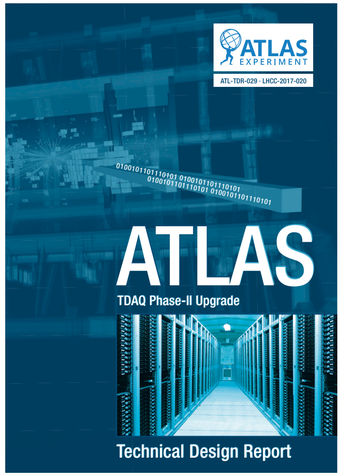


Tile
Calorimeter
ATL-TDR-028
300 pages



Y. Horii: editor
M. Corradi: main editor and 1st project leader

Muon
ATL-TDR-026
408 pages



Y. Horii: editor
M. Corradi: materials

Trigger & DAQ
ATL-TDR-029
608 pages

Another TDR provided and approved later for High-Granularity Timing Detector [ATL-TDR-031]

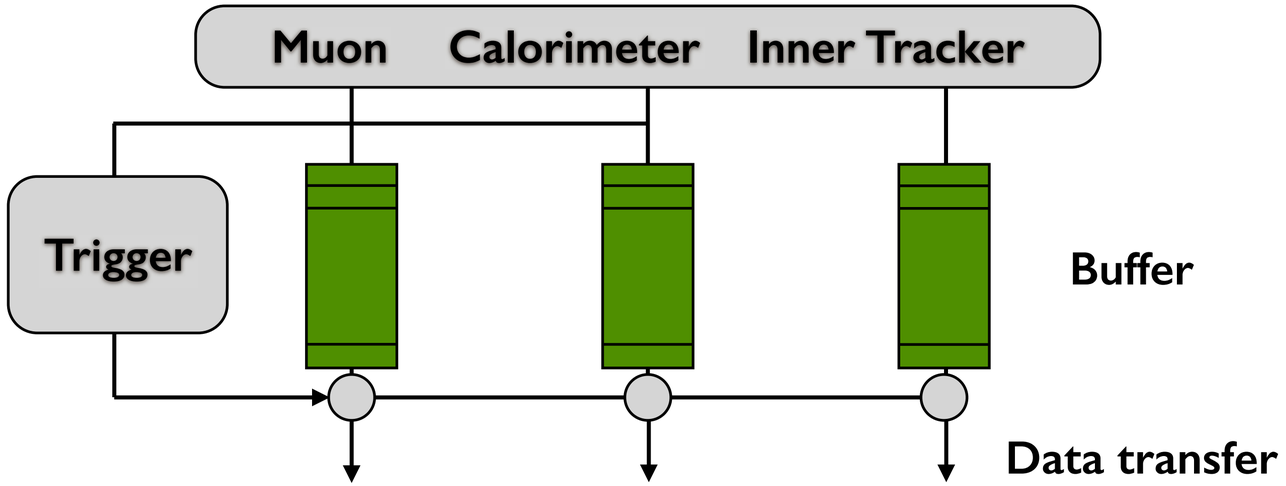
Upgrade of the Trigger and DAQ System

Extension of the trigger latency — improved selectivity

Extension of the trigger and event filter rates — more events to later stages

	LHC ATLAS	HL-LHC ATLAS
Trigger latency	2.5 μs	10 μs
Trigger output	100 kHz	1 MHz
Event filter output	1 kHz	10 kHz

Electronics upgrades are essential for the extensions of the latency and rate

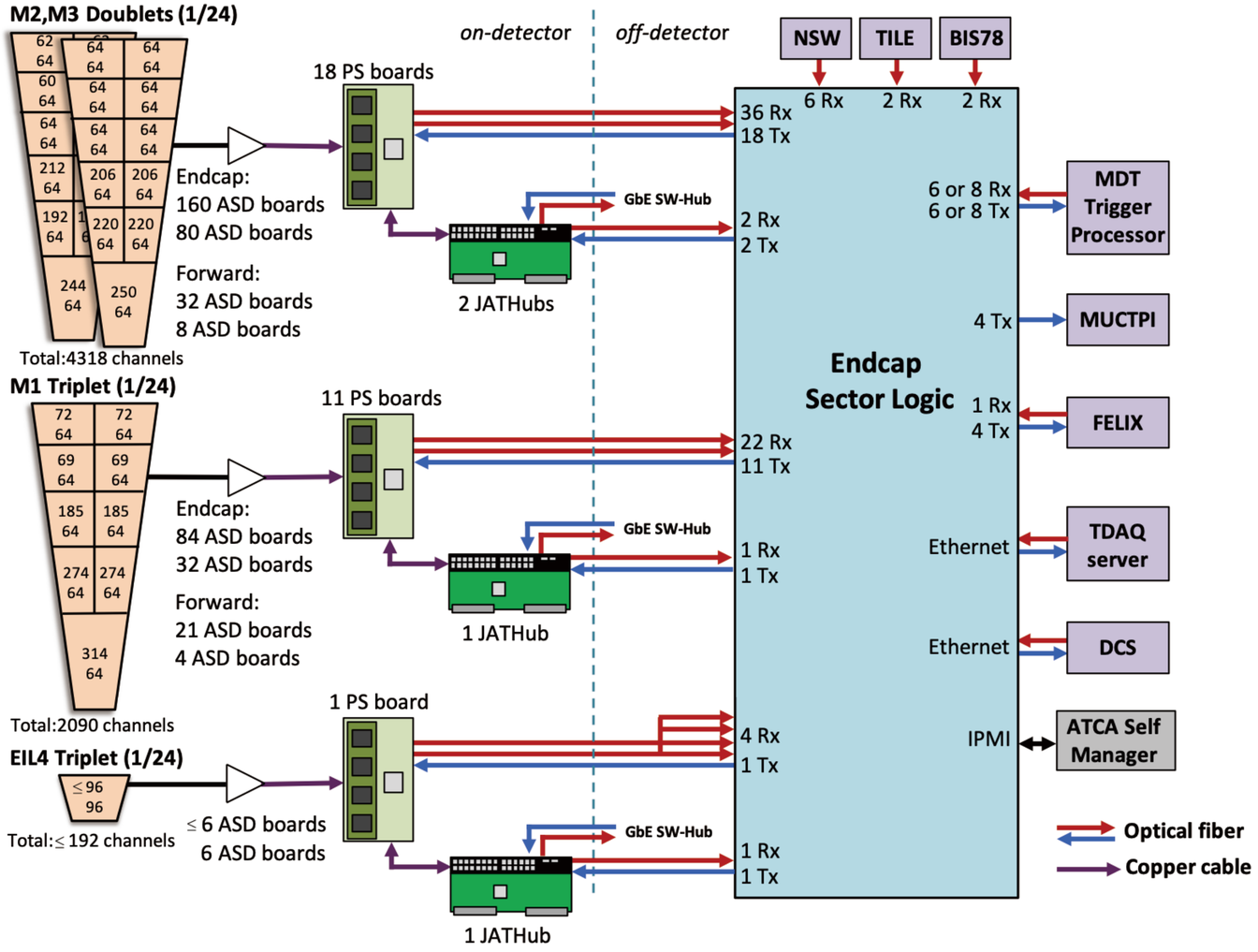


TGC Electronics for HL-LHC

All TGC electronics boards will be replaced except for the ASD boards.

All hit data will be transferred from on-detector boards (PS boards) to off-detector boards (SL boards).

Muon tracks are reconstructed in modern FPGAs on SL boards.



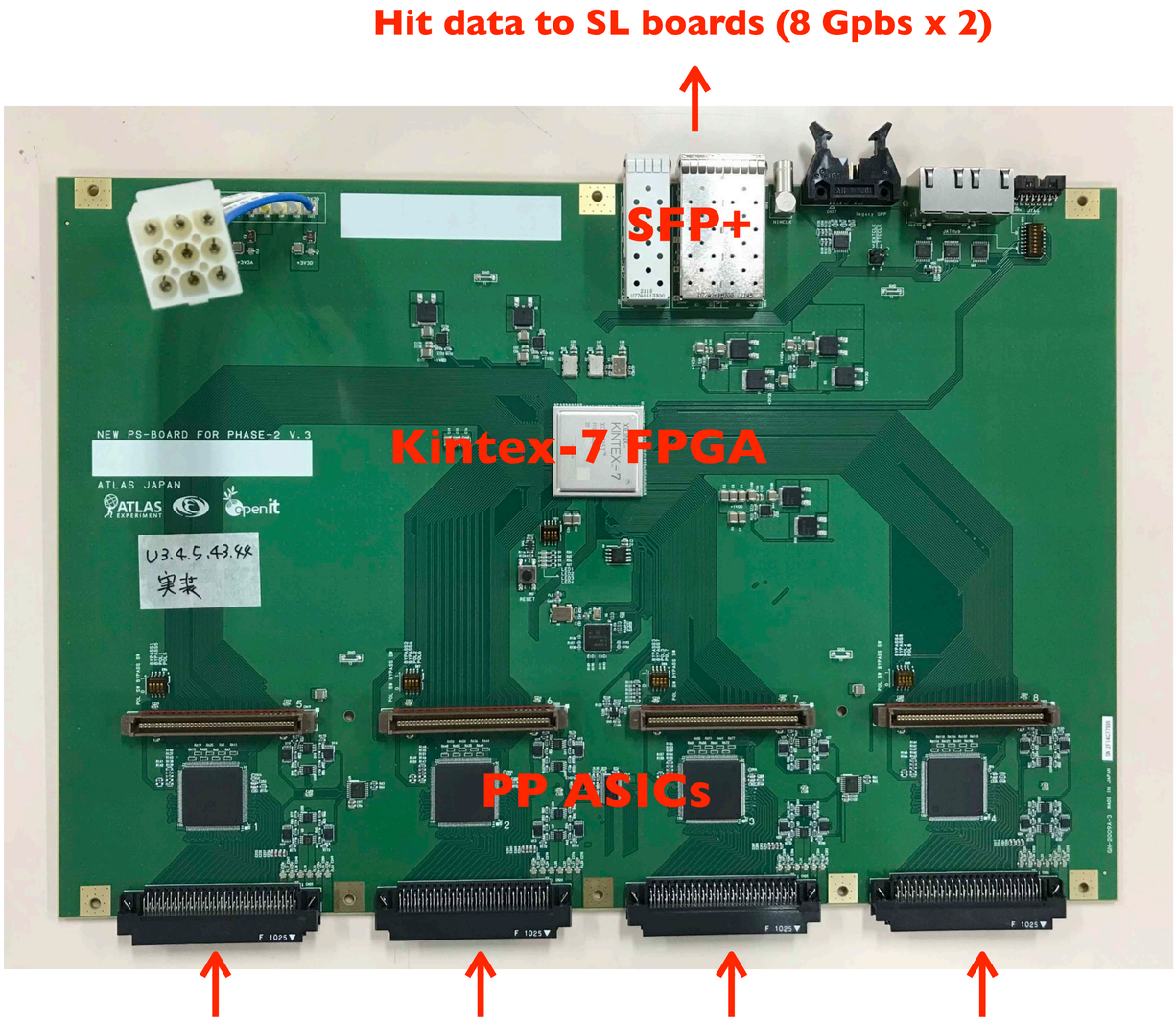
TGC System for HL-LHC

	Numbers
Detector channels	320k
ASD boards	23k
PS boards	1434
JATHub boards	148
SL borads	48

} Newly developed

PS Board — Overview

- PP ASIC receives the LVDS hit signals from the ASD boards and align the timing. Each hit is assigned to a bunch crossing.
- FPGA collects the hit data of 256 channels and transfers them to SL boards with 8 Gbps x 2 optical connections.
- FPGA controls the ASD boards and the components on the PS boards.
- ~7 W (1 board), ~10 kW (all boards)



Pre-production started in 2021

PS Board — Challenge

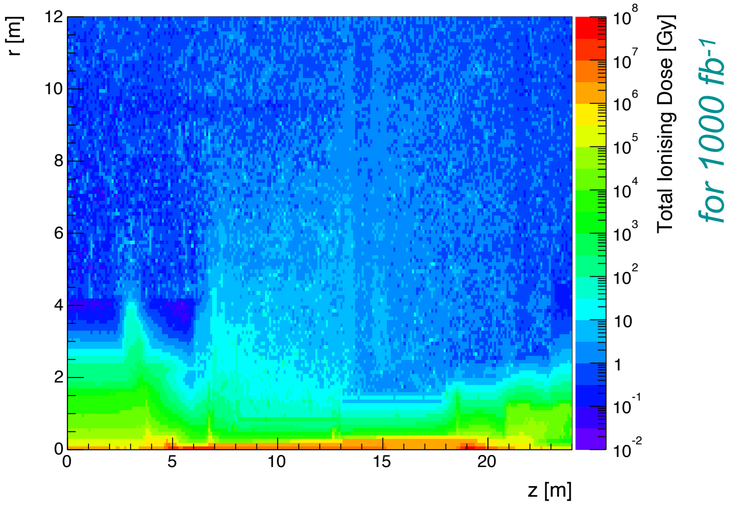
In order to establish a robust system, we use commercial-off-the-shelf (COTS) products for PS boards wherever possible.

Challenge: confirmation of the radiation tolerance of COTS products!

Simulation of radiation level

(Total Ionising Dose, TID)

PS board: 6 Gy at HL-LHC



Safety factors

- SF_{sim}: safety factor for simulation uncertainty
- SF_{ldr}: safety factor for low-dose rate at actual experiment
- SF_{lot}: safety factor for lot-to-lot difference and difference in lot

SF_{sim}			SF_{ldr}				SF_{lot}	
TID	NIEL	SEE	TID (COTS)	TID (ASICs)	NIEL	SEE	All (COTS)	All (ASICs)
1.5	2	2	1–5	1–1.5	1	1	1–4	1–2

Example: SF for FPGA TID: 1.5 x 5 x 4 = 30, requirement: 180 Gy

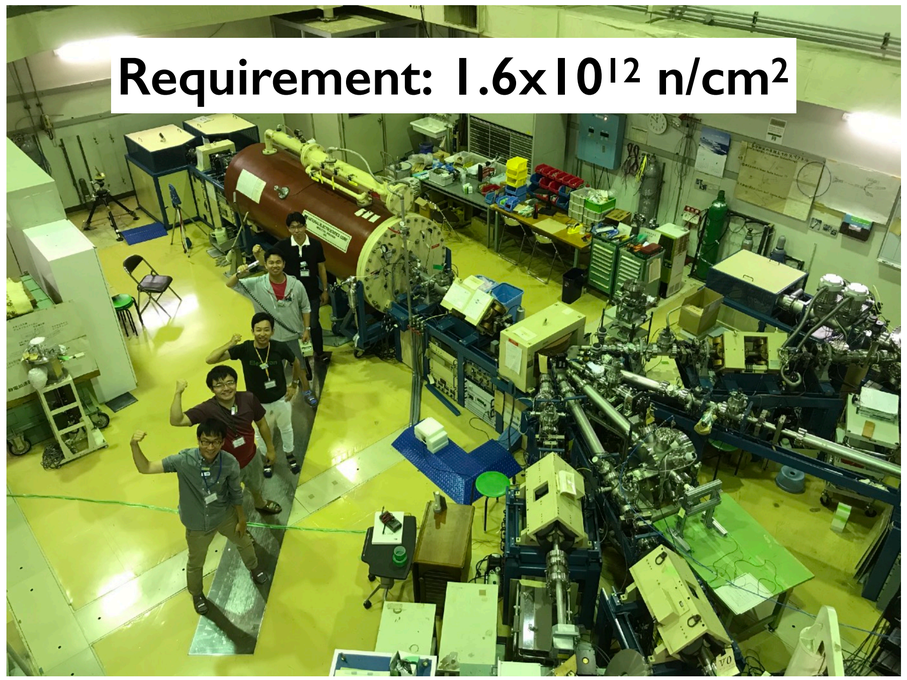
PS Board — Radiation Tests

Total Ionising Dose (TID)

Gamma irradiation test
at Nagoya Univ. (16 weeks)

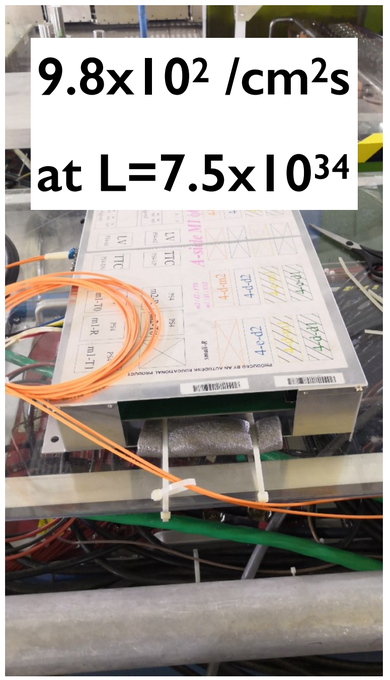
Non-Ionising Energy Loss (NIEL)

Neutron irradiation test
at Kobe Univ. (6 weeks)



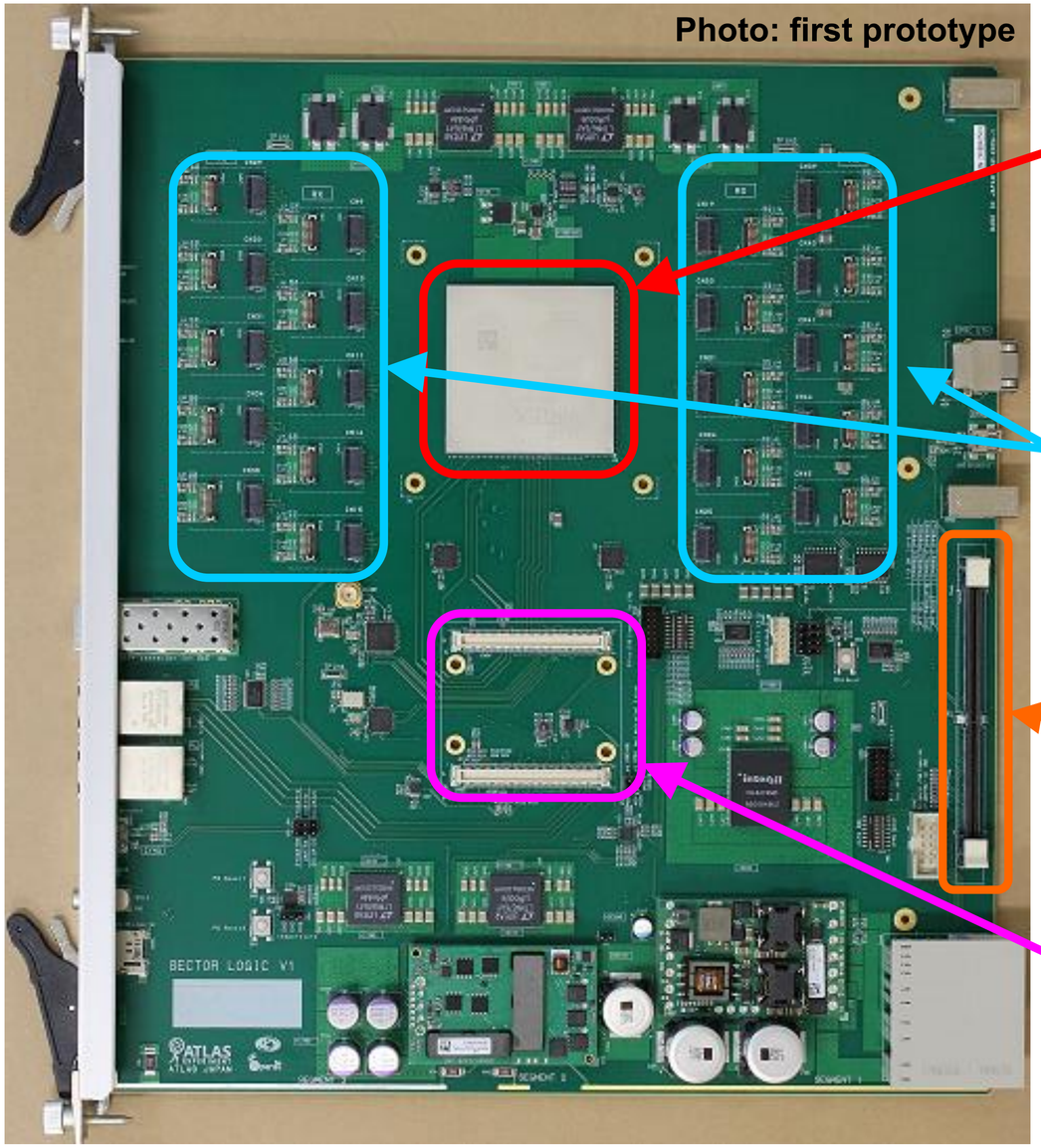
Single Event Upset (SEU)

SEU measurements and
recovery Demo. at CERN



Nagoya leaded and completed intensive radiation tests!

SL Board — Overview



Large-scale FPGA
- Xilinx XCVU13P
- Trigger and readout functions
- Control/monitor on-detector boards

Optical transceiver
- 120 pairs of TX and RX lanes of FireFly
- Receive detector signals and transmit trigger and readout outputs

IPMC mezzanine card
- CERN-developed IPMC
- Control/monitor power supply

MPSoC mezzanine card
- Enclustra Mercury XU5
- Control/monitor the FPGA

Form factor: ATCA

SL Board — Prototyping

First prototype tested:

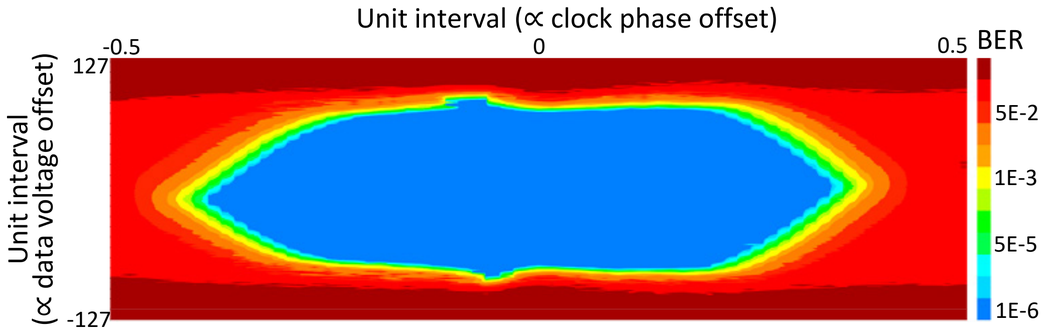
- Power up/down sequencing
- Temperature monitoring
- FPGA configuration and initial trigger firmware test
- FireFly loopback
- MPSoC-FPGA connection
- IMPC-Shelf manager connection
- Clock recovery for fixed latency (zero delay mode of Si5345)

Second prototype development in 2023

TWEPP 2022

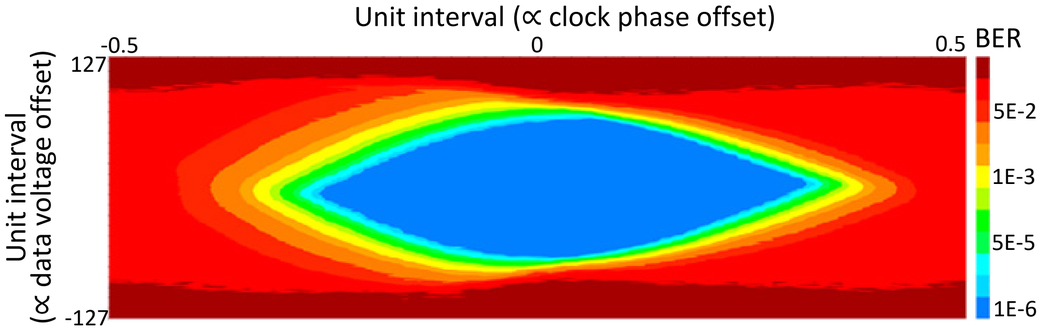
Result of FireFly loopback test with Xilinx IBERT

9.6 Gb/s assumed max rate for SL



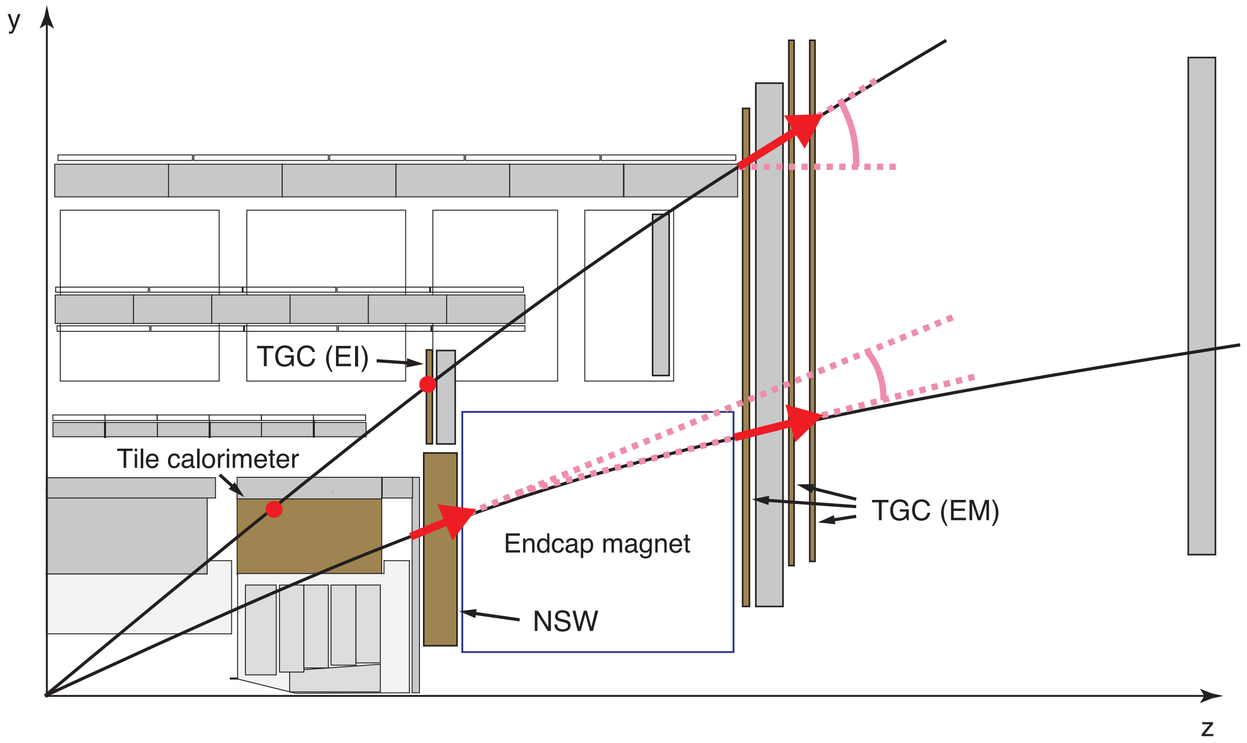
Nominal point (dedicated measurement):
BER < 3.4×10^{-15} (95 % C.L.)

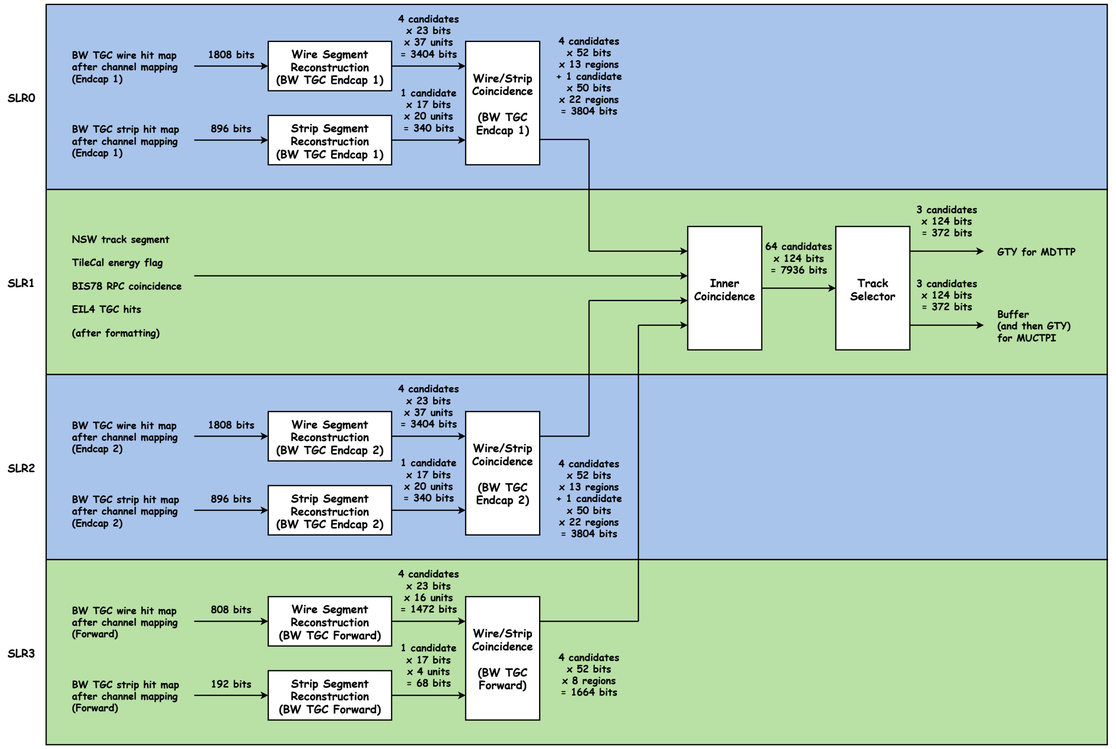
18.0 Gb/s as a test of board capacity



$$\text{BER (Bit Error Ratio)} = \frac{\text{Number of error bits}}{\text{Number of transferred bits}}$$

Fast Muon Reconstruction — Design





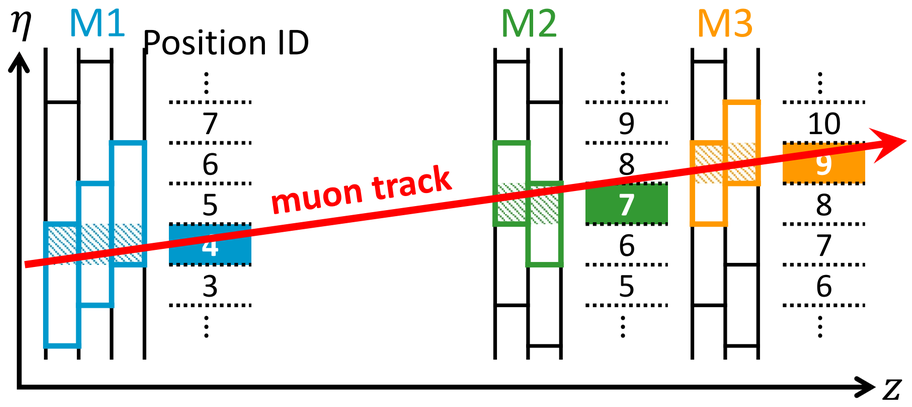
Muon tracks reconstructed from TGC (EM) and selected with inner detectors.

Fast Muon Reconstruction — Firmware

Pattern matching — ultimate method (concept: M. Tomoto, firmware design: Y. Horii)

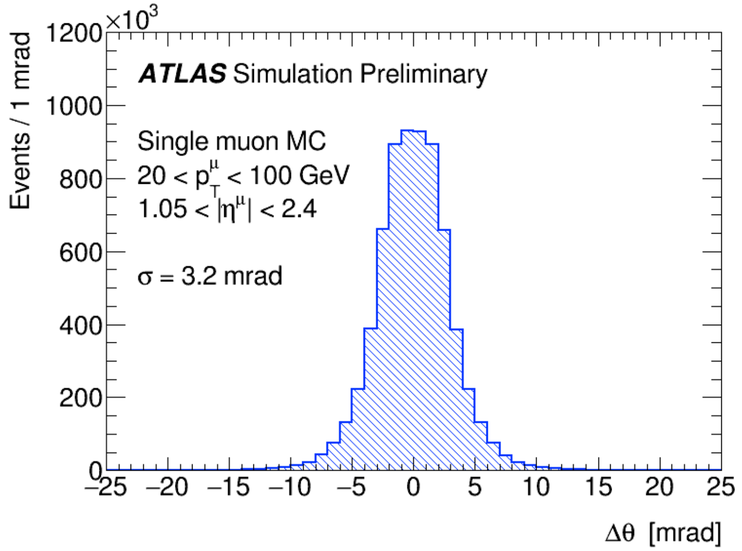
①Take coincidence and output position IDs in each of three stations: M1 (3 layers), M2 (2 layers) and M3 (2 layers)

②Combine position IDs on three stations and obtain segment data from FPGA UltraRAM where segment data are stored



Hit pattern list stored in UltraRAM

Position ID			Track segment (position, angle)
M1	M2	M3	
4	7	8	η_1, θ_1
4	**7**	**9**	$\boldsymbol{\eta_2, \theta_2}$
4	7	10	η_3, θ_3



https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L0MuonTriggerPublicResults#Performance_of_trigger_algorithm

Fast Muon Reconstruction — New Method (I)

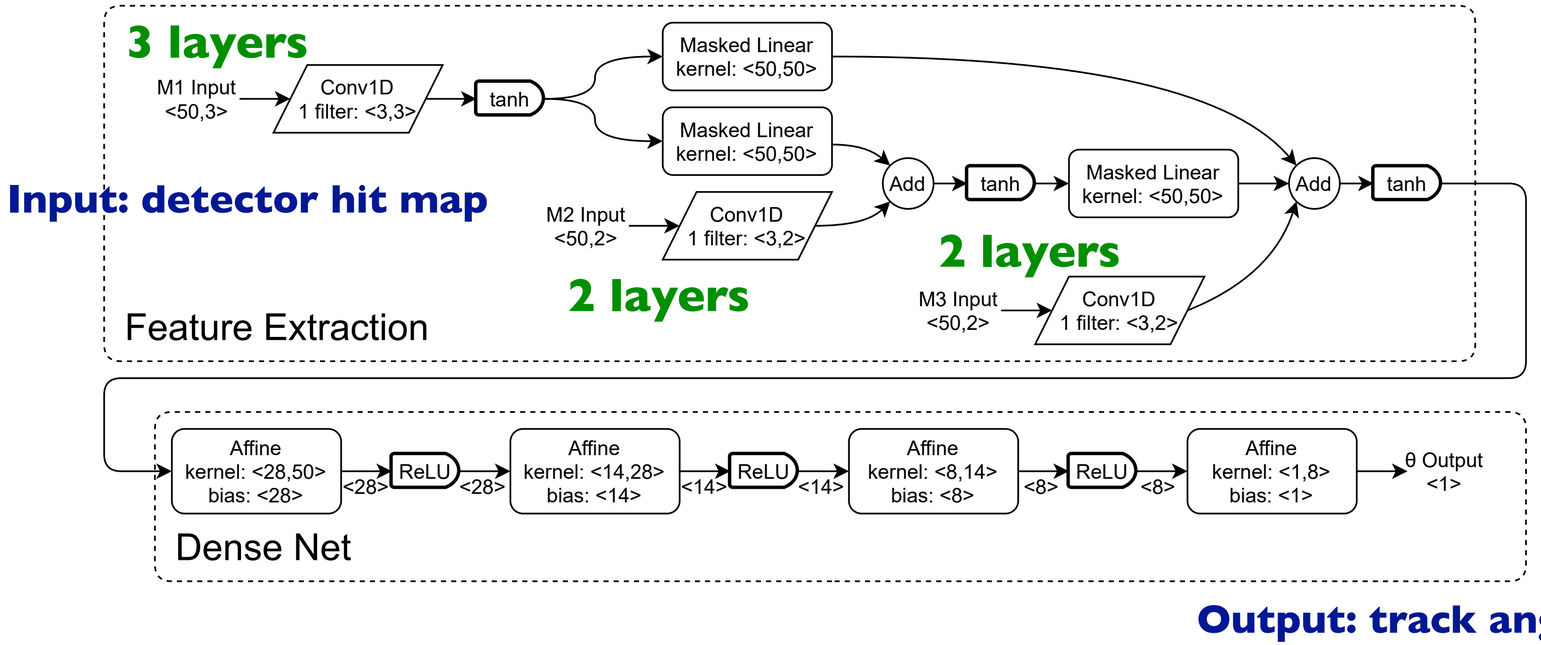
Fast muon reconstruction developed with machine learning (CNN) implemented in FPGA

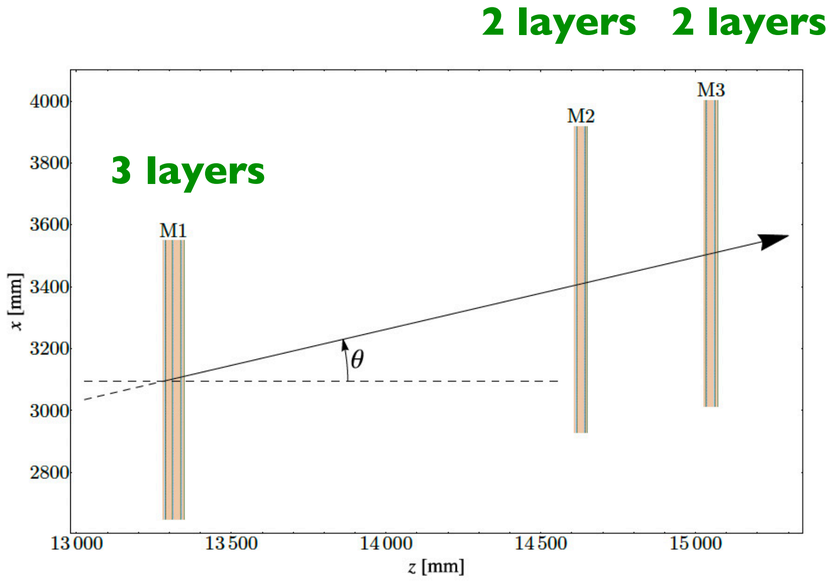
The workflow shown in the following

	Software simulation		Firmware simulation		FPGA implementation
Tool	Keras + TensorFlow	hls4ml	Vivado™ HLS	VIVADO	
Purpose	ML training . json : model structure . h5 : weight	Convert to C/C++	Convert to Verilog/VHDL	Implementation	Performance evaluation

Fast Muon Reconstruction — New Method (2)

A compact CNN developed — the structure optimised for the TGC detector, the parameters quantised, highly sparse network provided by pruning

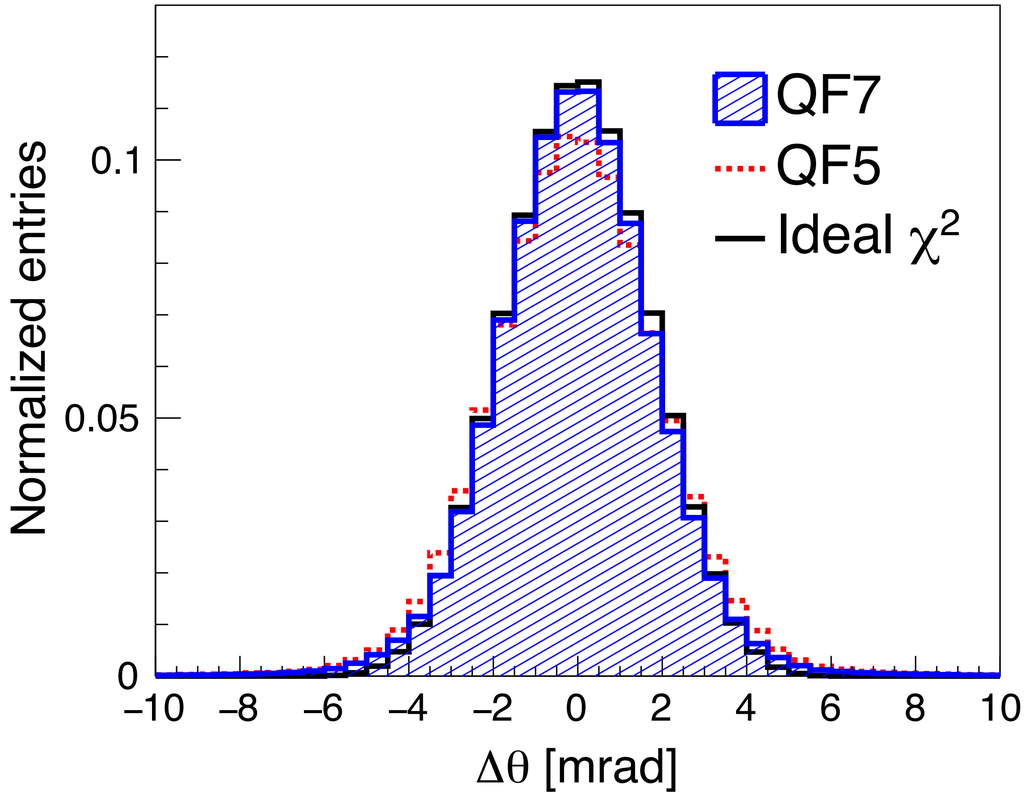




Fast Muon Reconstruction — New Method (3)

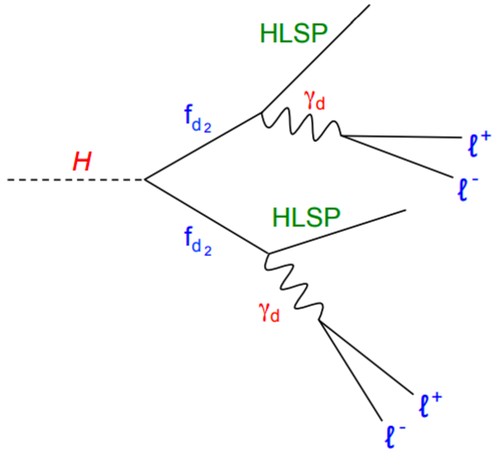
- Successfully implemented in XCVU13P FPGA
- Angular resolution similar to minimum χ^2
- Latency < 100 ns

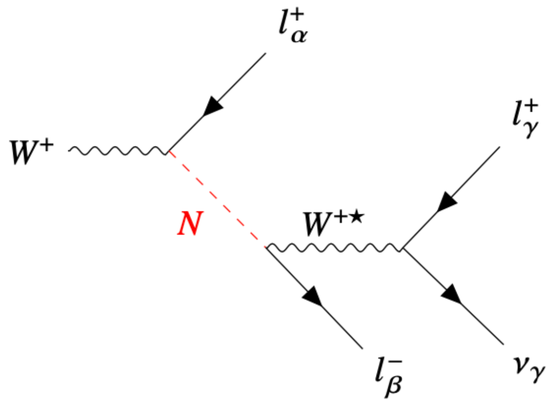
NIMA 1045, 167546 (2023)

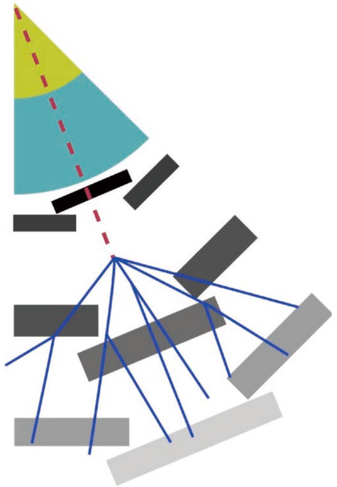


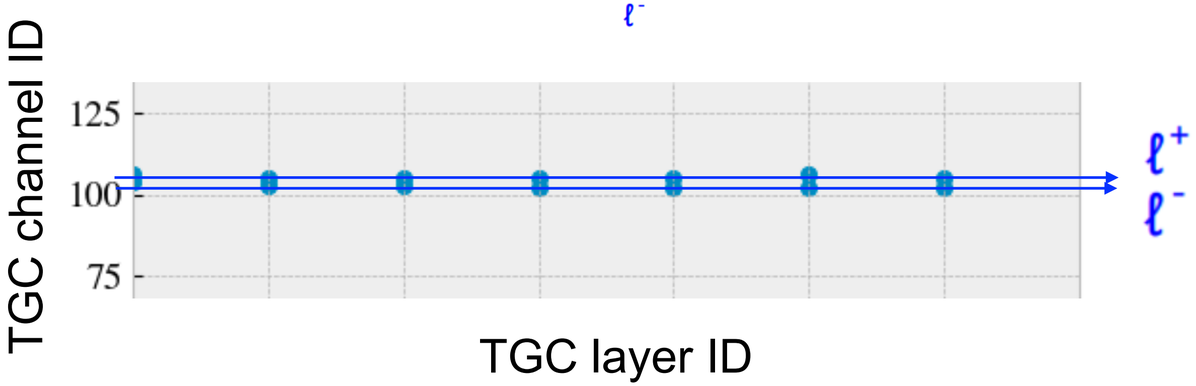
Possible Future Extensions

The algorithms with machine learning could extend the trigger acceptance for exotic signatures, e.g. close-by leptons, lepton jets, …









Study ongoing…

Summary

- The ATLAS experiment will be upgraded to fully exploit the physics potential of HL-LHC.
- The TGC electronics will be replaced for larger latency and rate of the first-level trigger. All TGC data will be transferred to off-detector boards, and muon tracks are reconstructed in modern FPGAs.
- Fast muon reconstruction with a pattern matching method was developed as a baseline. Method with machine learning is under study.

Backup Slides

Physics Prospect for HL-LHC (Selected)

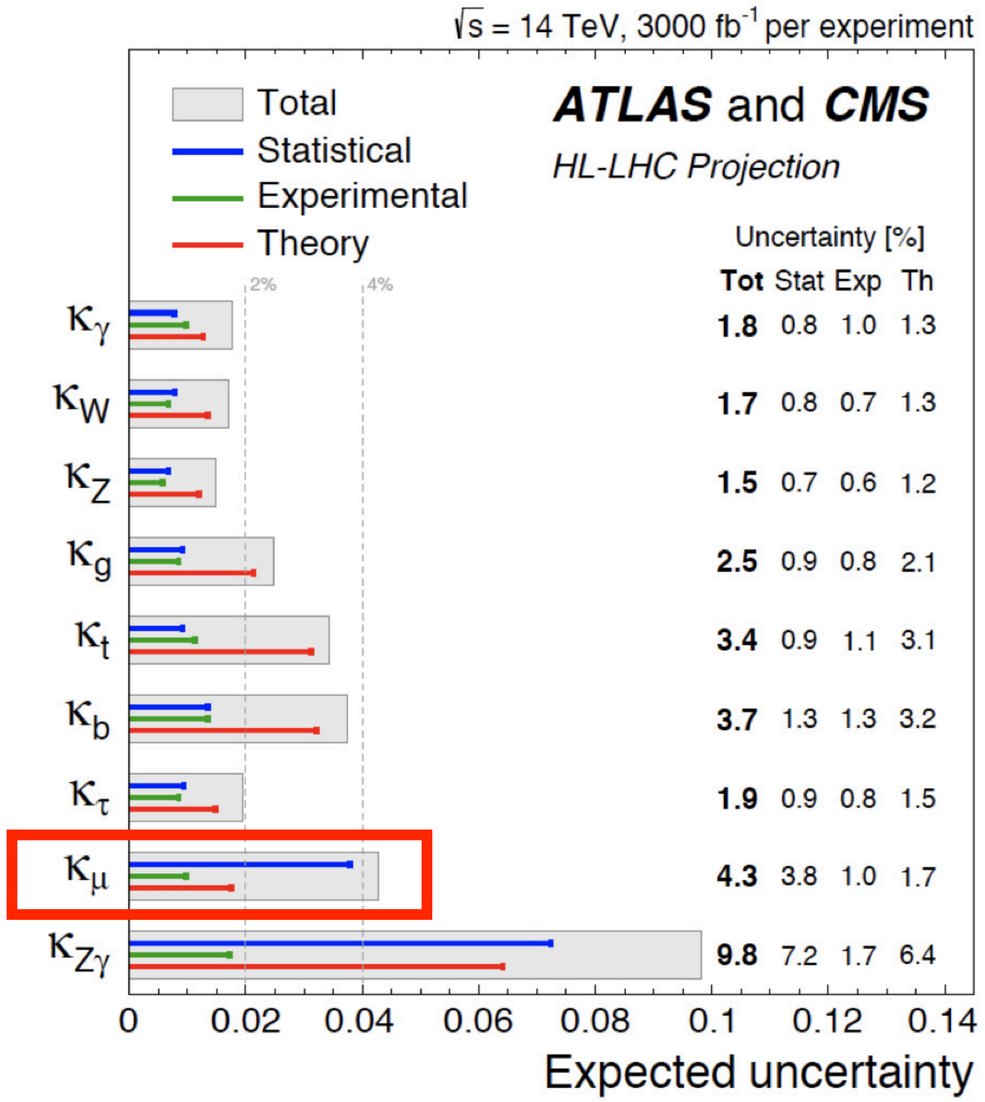
Improved measurements of the Higgs coupling

to gauge bosons and fermions

— improved understanding of the origin of masses

Percent-level for muon — second-generation fermion

CERN-LPCC-2018-04



Increase of Cross Section

Run 1: 7-8 TeV

Run 2: 13 TeV

Run 3: 13.6 TeV

LHC Design: 14 TeV

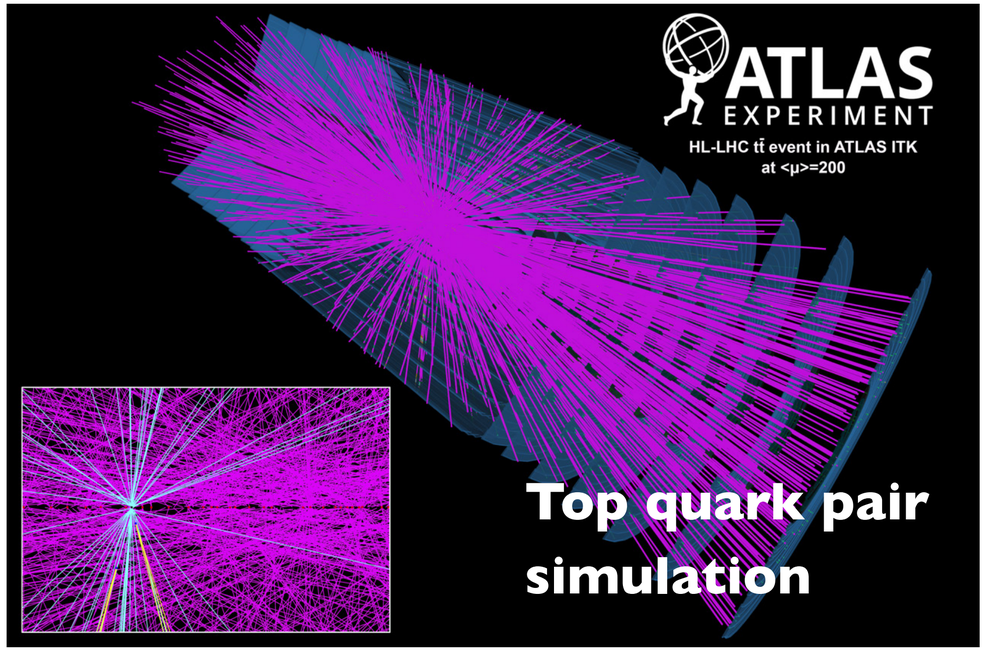
Channel	13.6 / 13 TeV	14 / 13.6 TeV
H (ggF)	7%	6%
HH	11%	7%
tt	11%	6%
ttH	13%	7%
tttt	19%	11%
SUSY stop (1.2–1.5 TeV)	20–30%	14–19%
Z' (5–6 TeV)	50–70%	30–40%
QBH (9.5 TeV)	250%	100%

Increase of cross section — large for high mass

Challenges for HL-LHC

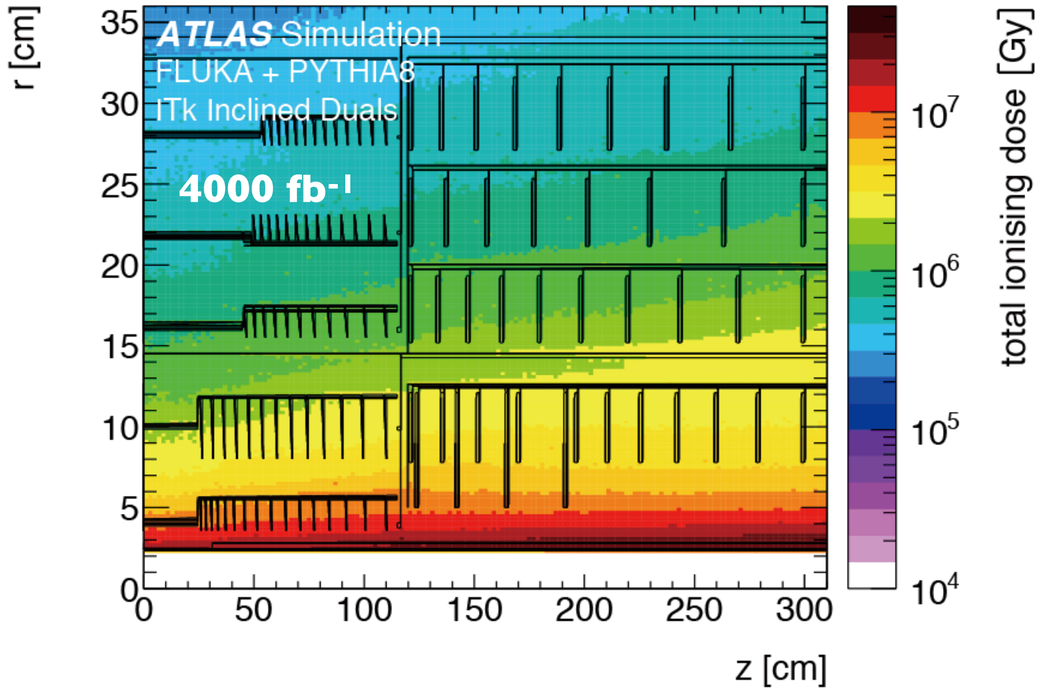
High luminosity, high pileup (high number of proton-proton collisions per proton-bunch crossing), high radiation level

Pileup 200

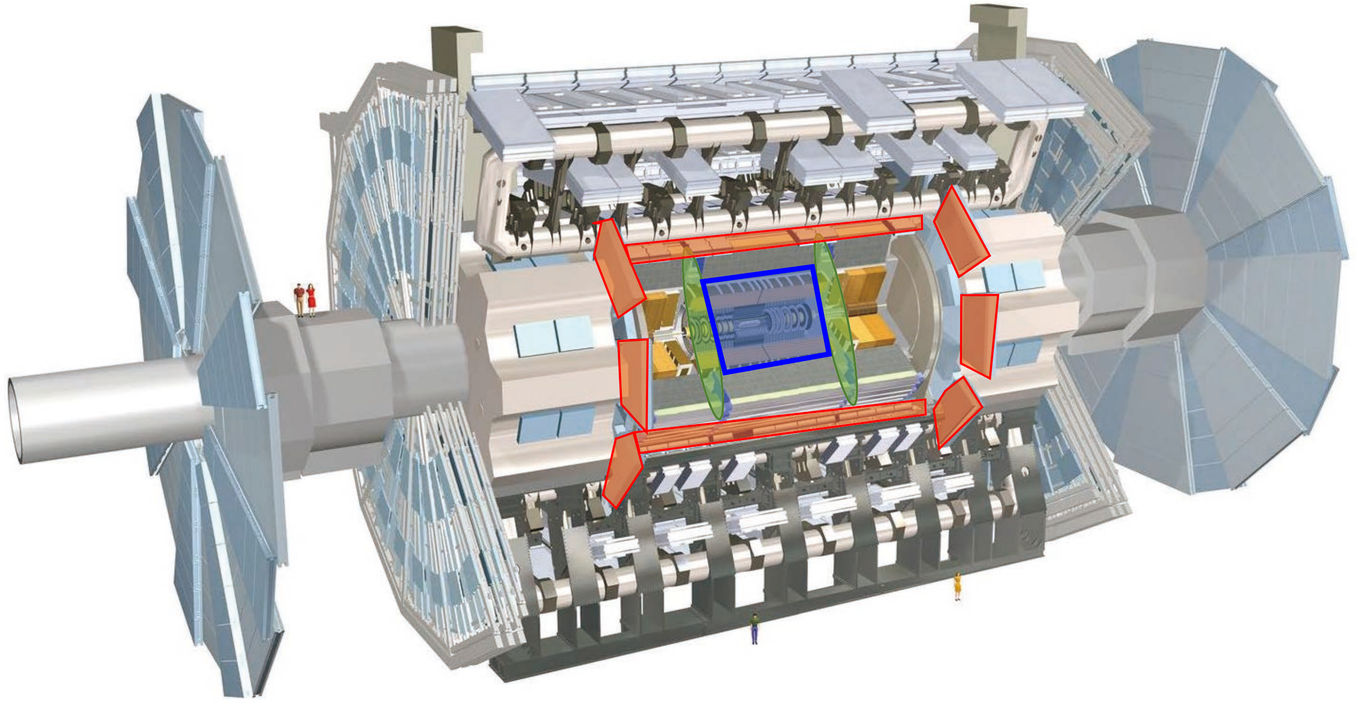


Total Ionising Dose: maximum 20 MGy

1 MeV neutron Eq. flux: maximum 2.6 x 10^{16} cm^{-2}



ATLAS Upgrades for HL-LHC



New Inner Tracking Detector

- All silicon with at least 9 layers up to $|\eta| = 4$
- Less material, finer segmentation

New Muon Chambers

- Inner barrel region with RPCs, sMDTs, and TGCs
- Improved trigger efficiency/momentum resolution and reduced fake rate

High Granularity Timing Detector (HGTD)

- Precision time reconstruction (30 ps) with Low-Gain Avalanche Detectors (LGAD)
- Improved pileup separation

Upgraded Trigger and DAQ System

- Single level trigger at 1 MHz
- Improved 10 kHz event farm

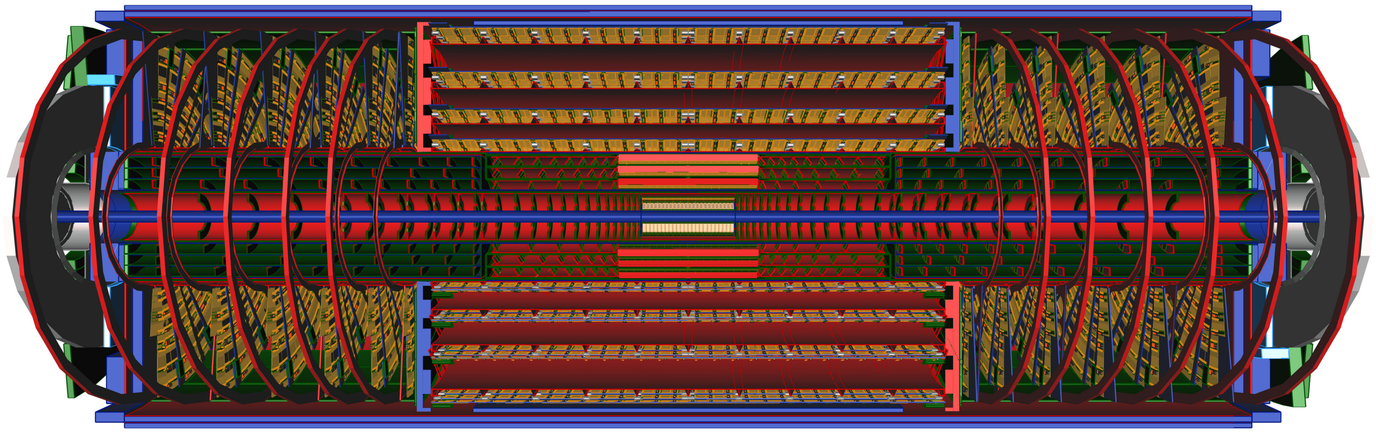
Electronics Upgrades

- On-detector/off-detector electronics upgrades of LAr Calorimeter, Tile Calorimeter, and Muon Chambers
- 40 MHz continuous readout with finer segmentation to trigger

New Inner Tracking Detector

- 178 m^3 of silicon pixel + strip — factor of 2.7 larger than the current ATLAS
- Finer segmentation — improved vertexing, tracking, jet flavour tagging, …
- Coverage increased from $|\eta| < 2.5$ to $|\eta| < 4$

η: pseudorapidity



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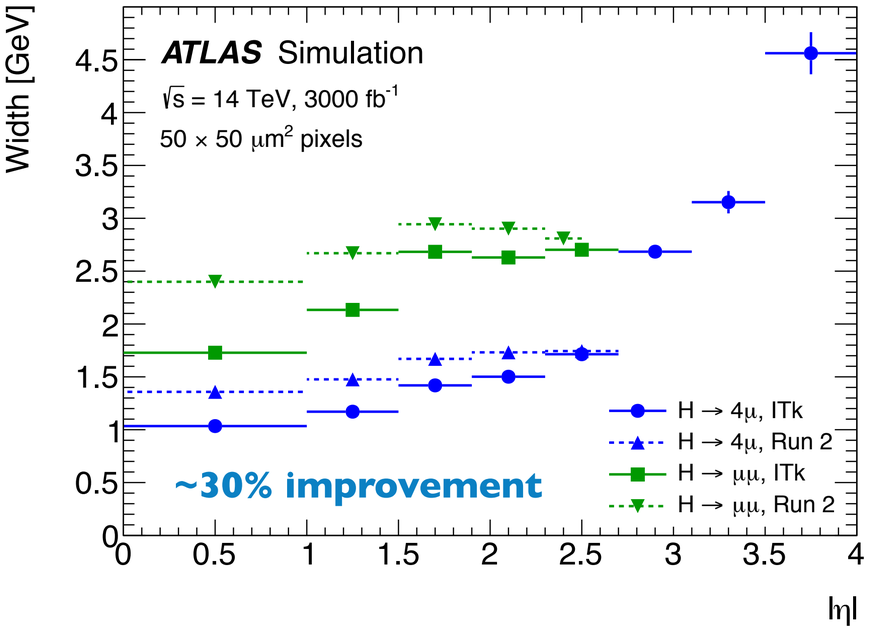
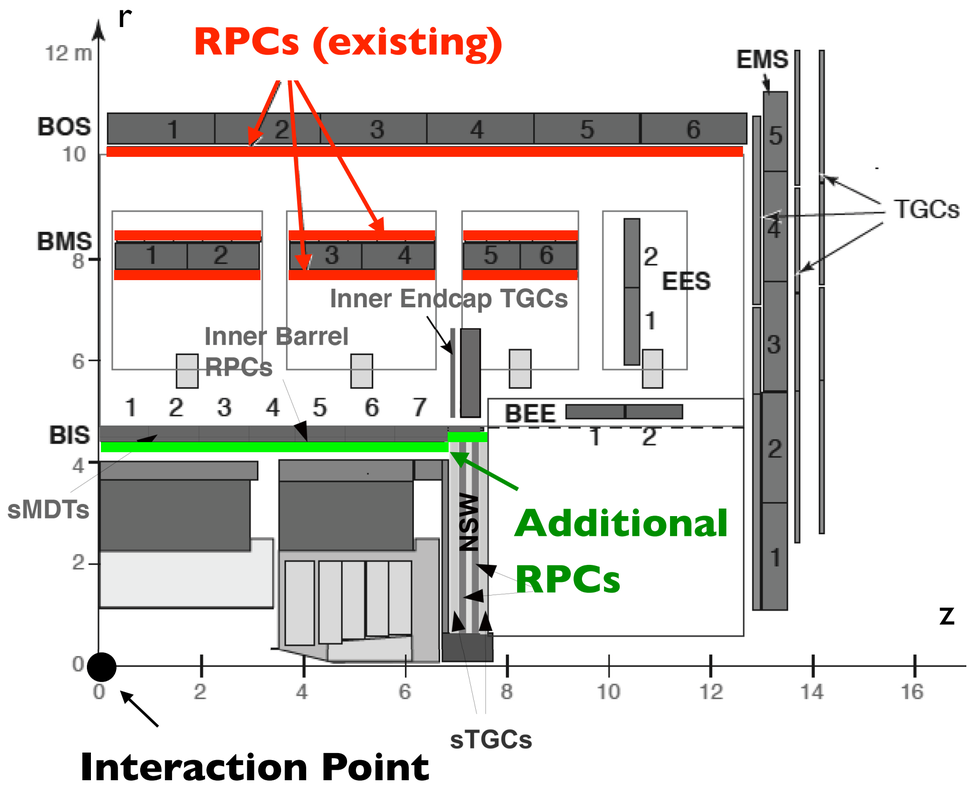
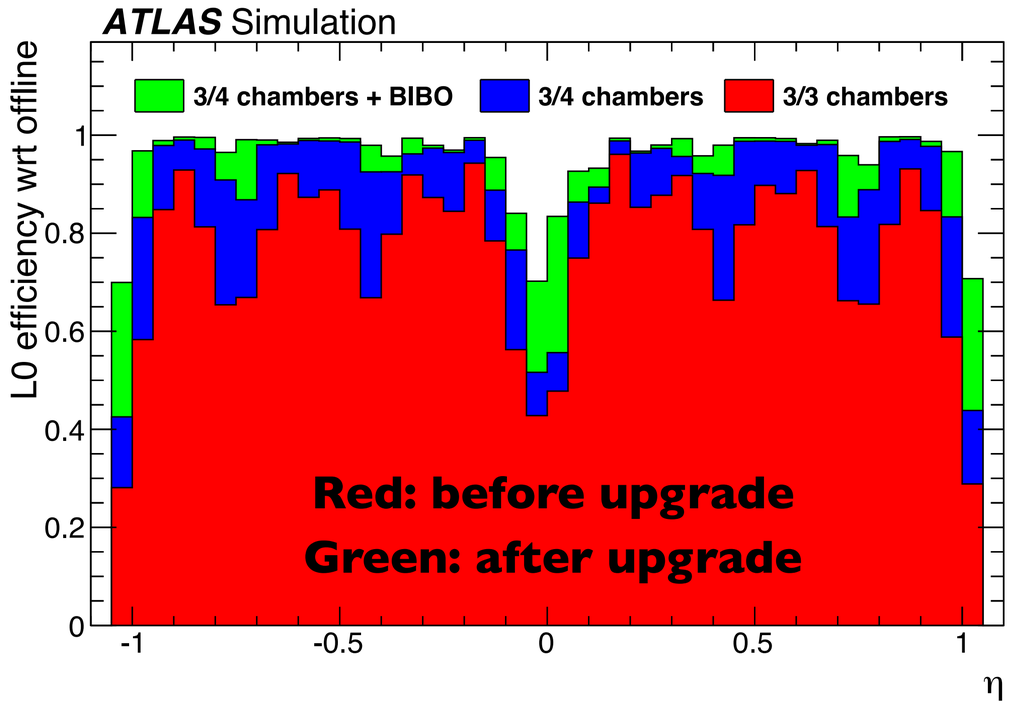


New Muon Chambers

- **Acceptance of the muon trigger in the barrel region improved by additional Resistive Plate Chambers (RPCs): 78% → 96%**

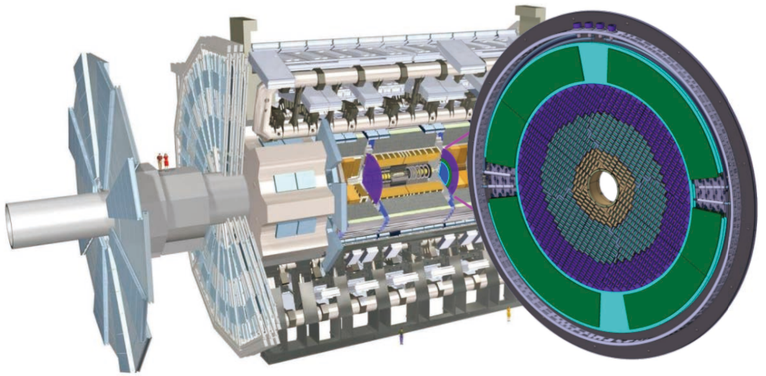
- Monitored Drift Tube (MDT) in the barrel inner layer replaced by small-diameter MDT for free space for RPCs.
- Doublet Thin Gap Chambers (TGCs) in the endcap inner layer replaced by triplet TGCs for fake reduction.

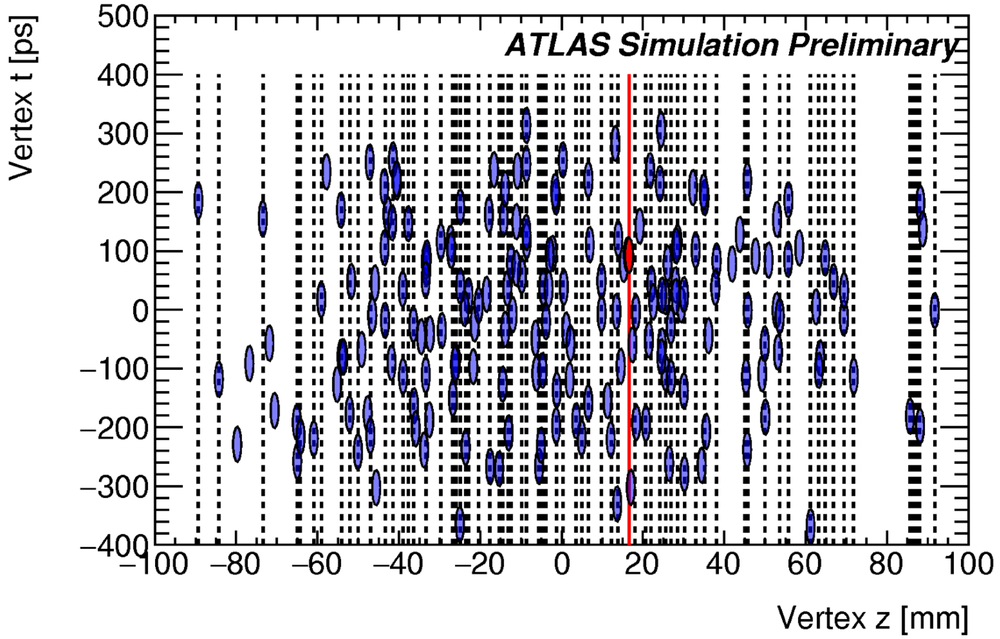


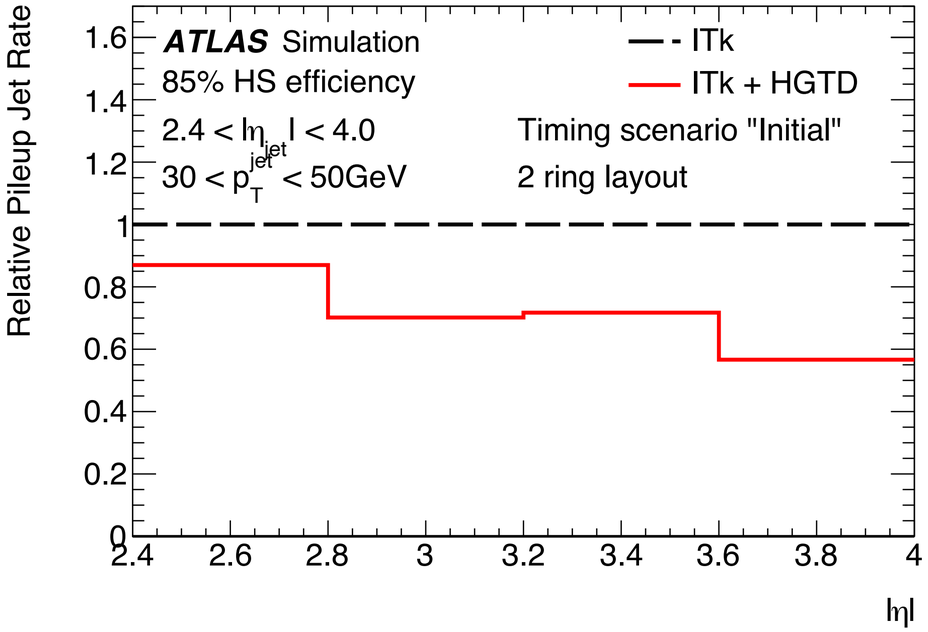


High Granularity Timing Detector

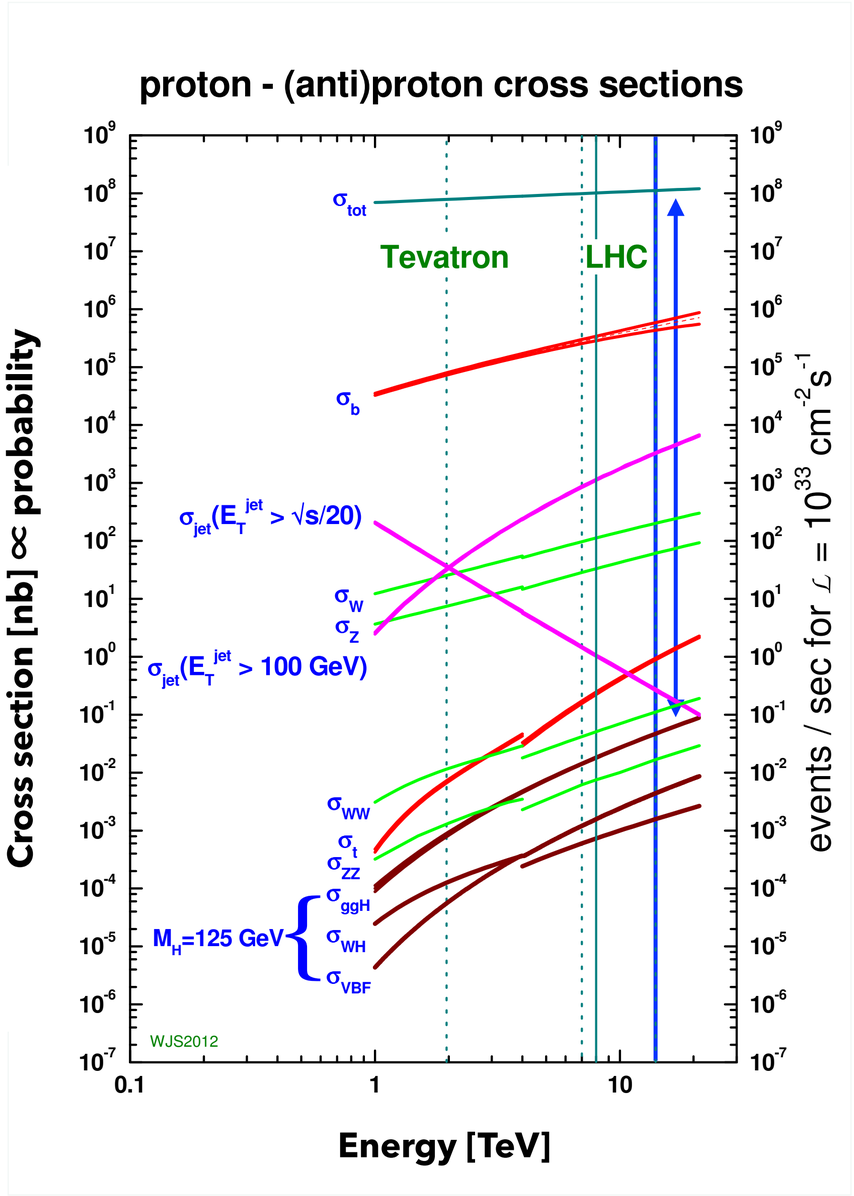
- Precision time reconstruction (30 ps) with LGAD
- Coverage: 2.4 < |η| < 4.0
- Pixel size: 1.3 x 1.3 mm², thickness: 50 µm
- Improved pileup jet suppression







Cross Section and Trigger

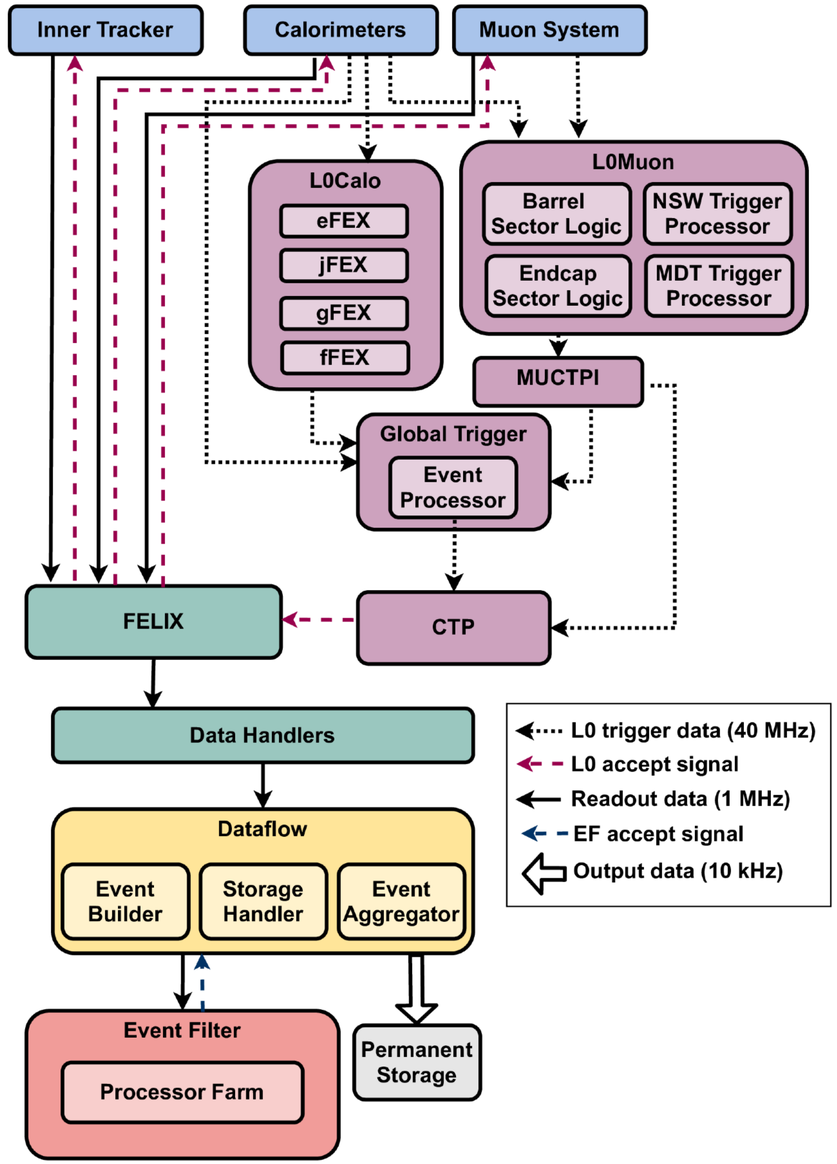


The cross section of the Higgs boson production is only 0.0000000005 of the total cross section of the proton-proton collision…

We select interesting collisions before storage — “trigger”.

Trigger and DAQ Upgrade

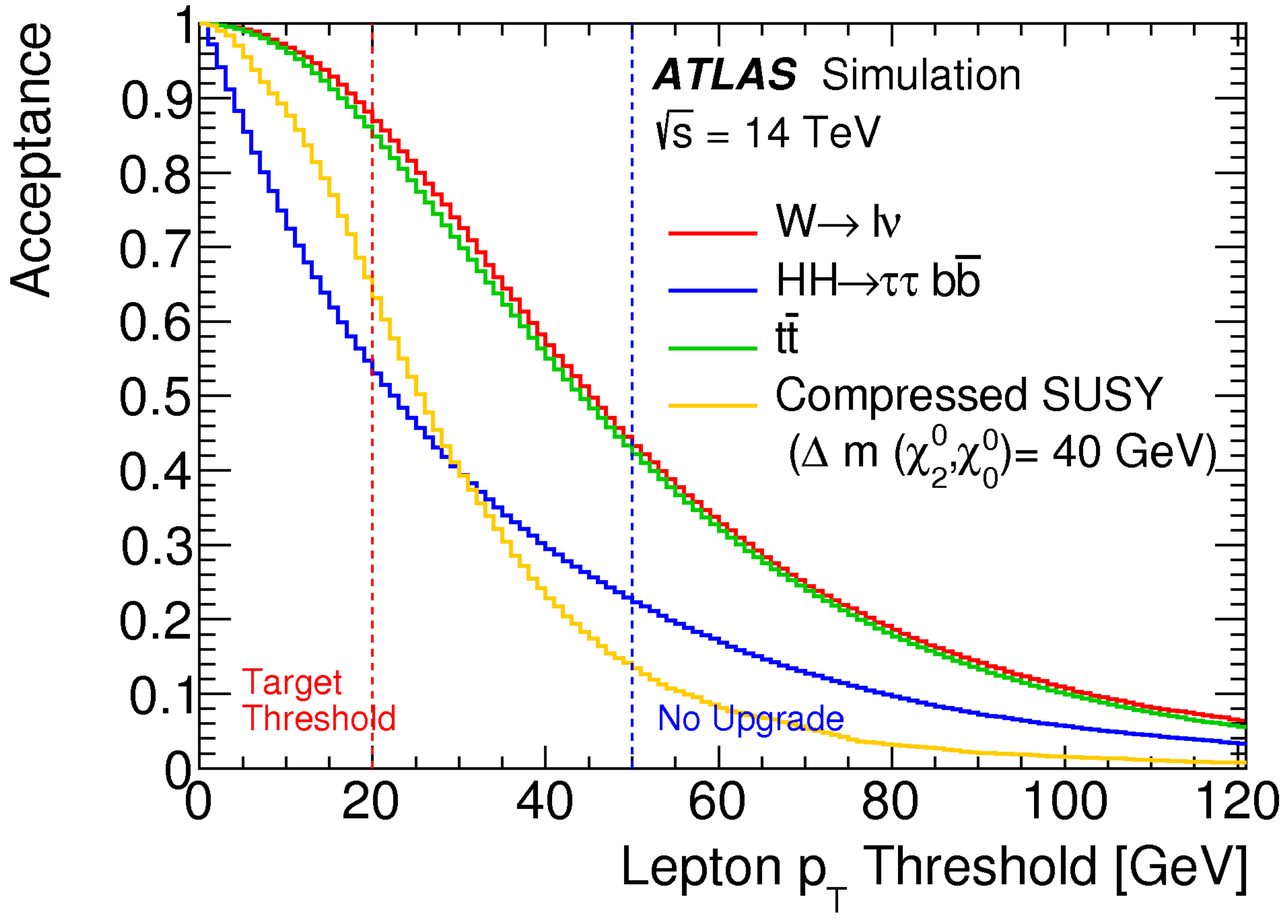
- Level 0: 1 MHz, ~5.2 TB/s, latency 10 μs
  - LHC: 100 kHz, ~290 GB/s, latency 2.5 μs
- Event Farm: 10 kHz, ~52 GB/s
  - LHC: 1 kHz, ~2.9 GB/s



Trigger and DAQ Upgrade

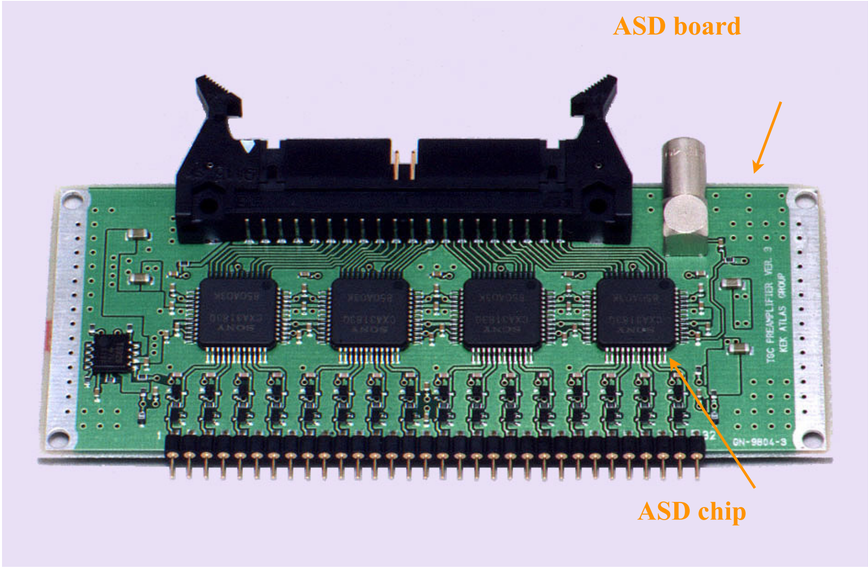
With the upgrade of the trigger and DAQ system, trigger thresholds similar to those used at Run 1 can be used at HL-LHC.

Retain high acceptance for various physics processes!

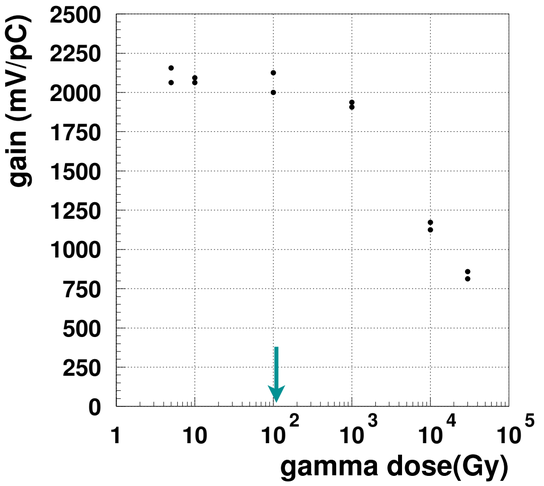


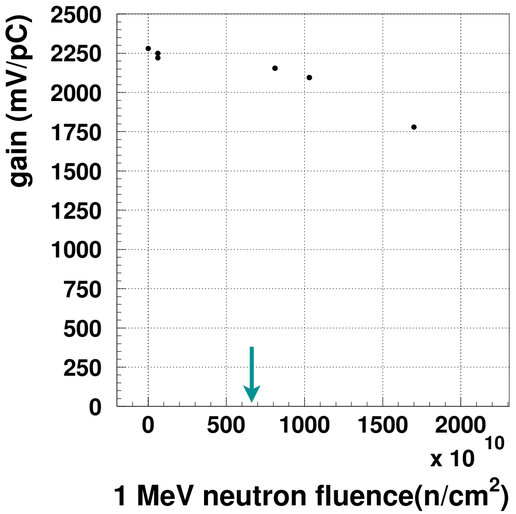
TGC ASD Board

- SONY analog master slice (bipolar)
- Preamplifier gain of 0.8V/pC
- Comparator with LVDS outputs
- ENC ~ 7500 electrons at C_{input} = 150 pF
- 16 channels per board

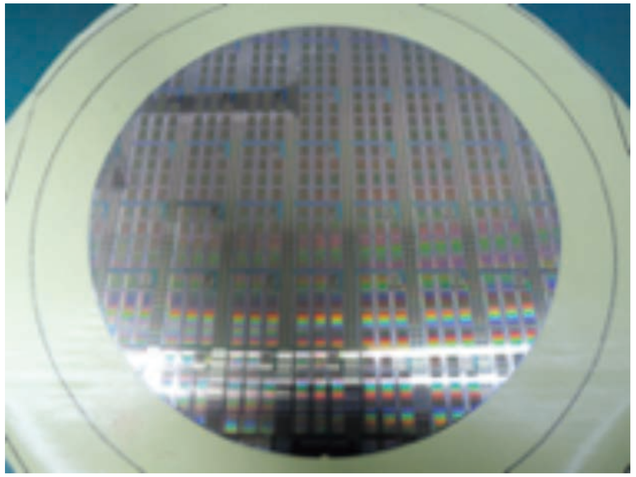


The current ASD chips satisfy the radiation tolerance criteria for HL-LHC. No replacement planned.

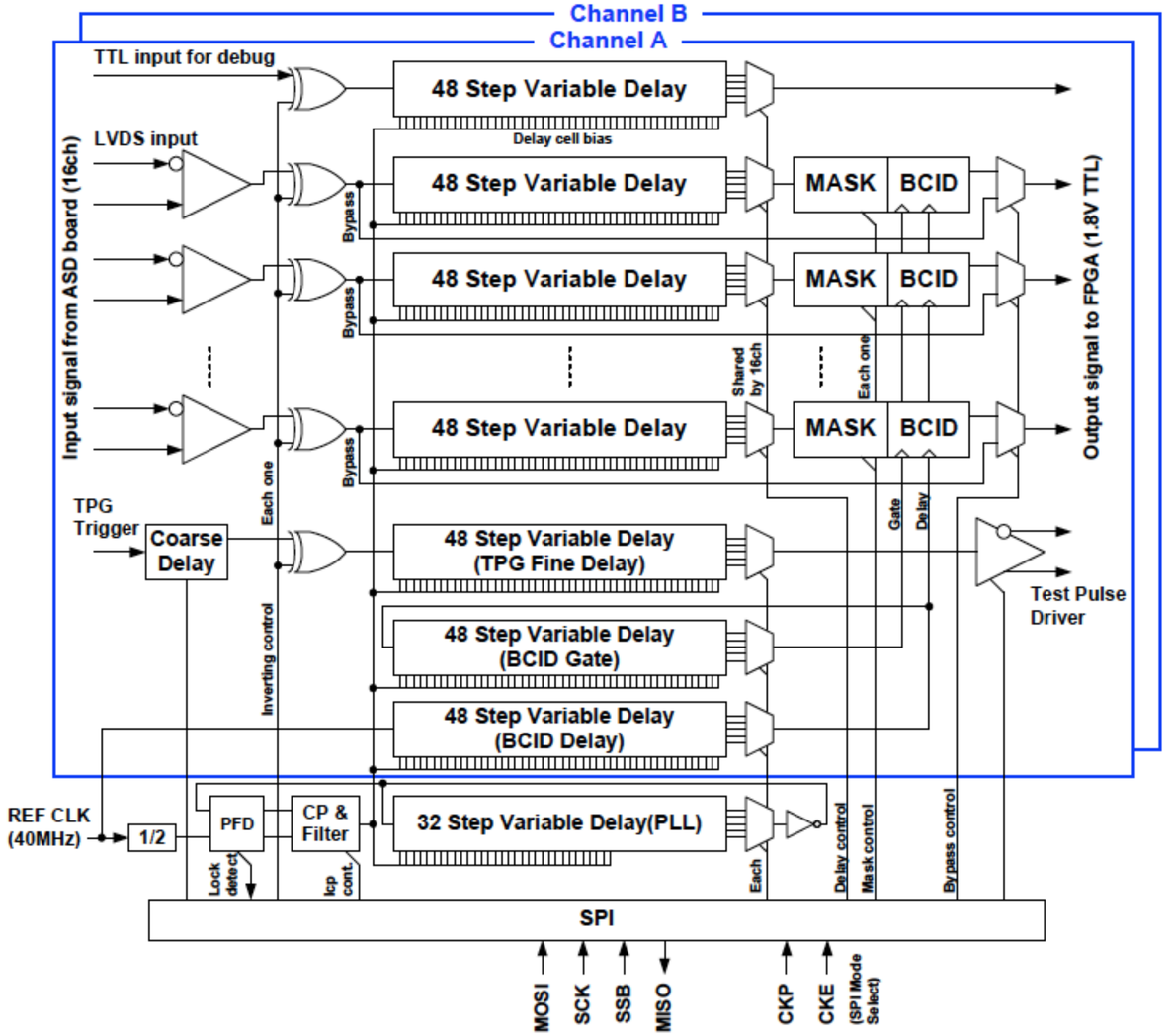




TGC PP ASIC

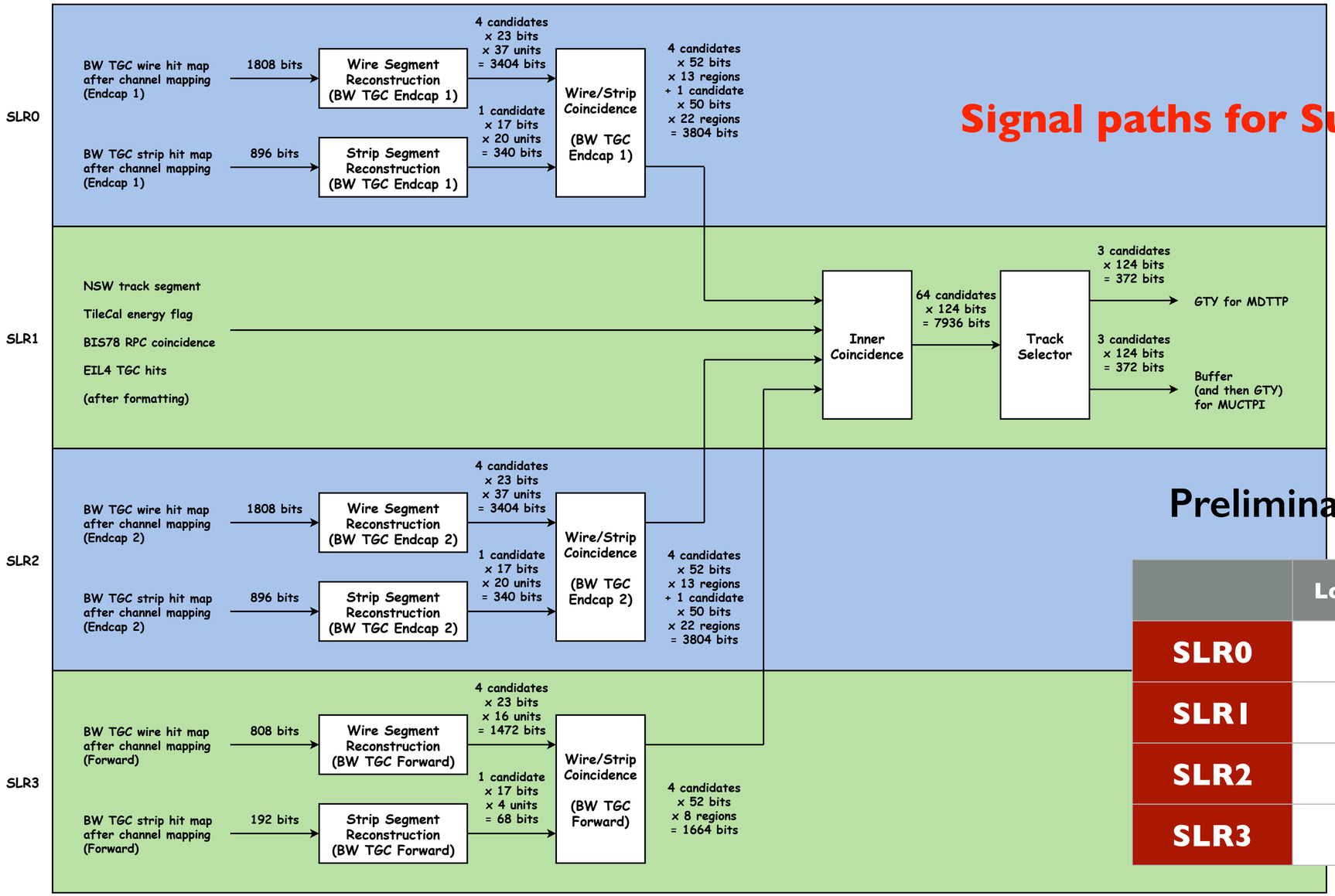


Design process	Silterra 0.18 μs CMOS 6M1P
Supply voltage	3.3 V (LVDS Rx, TPG Driver) 1.8 V (PLL, Delay line, CMOS input and output) Voltage tolerance : ± 10 %
# of channels	Group A (16 ch), Group B (16 ch)
Timing control resolution	< 1 ns
Timing control range	> 40 ns
Timing jitter	~40 ps (LVDS Rx), ~40 ps (Variable Delay)
Temperature range	0 ~ 80 ℃
Power consumption	~20 mW (Previous design: 130 mW)



Mass production completed.

TGC Fast Muon Reconstruction — Firmware



Signal paths for Super Logic Region (SLR)

Preliminary resource utilisation

	Logic cells	BRAM	URAM
SLR0	68%	22%	52%
SLR1	64%	36%	43%
SLR2	68%	22%	52%
SLR3	27%	10%	21%